As the separation between the atoms is reduced, the splitting of the 3s state into 2N levels and the splitting of the 3p state into 6N levels takes place. For example, the Splitting for distance R_1 of the 3s and 3p states into 2N and 6N levels respectively is shown in the figure. Here E_g is called the band gap.

Band gap is the difference between the maximum energy level of the E_s state and the minimum energy level of the Es state for the given inter atomic separation.

On further reduction in the inter atomic separation, there is no gap between 3s and 3p types of bands. From this separation onwards, we get a combined wave function, by carrying out the integration of the 3s and 3p type wave function. On further reducing the separation the two bands containing 4N energy level each are obtained. The band gap between them is shown in figure 5.4. The two bands for the equilibrium position of silicon is shown in the **figure 5.4.** As per Pauli's exclusion principle, we can have one electron for each energy level. As a result, the lower band will be completely occupied by 4 N number electrons. (As per Pauli's exclusion principle, each level cannot accommodate more than one electrons.) Here lower band is called valence band.

The upper band is completely empty. A minimum of E_g energy will have to be supplied to the electron to move from the valence band to the upper band. It can move in to any of the energy levels in the upper hand, since it is completely empty. If it does so it becomes a free electron and is available for electrical conductions. It is for this reason the upper band is known as the conduction band.

The difference in the lowest energy of the conduction band and the maximum energy of the valence band is known as band gap (E_g).

There are no available energy states in the band gap. It is for this reason that this gap is known as forbidden gap.

5.2.2 Classification of solid substances in reference to Band theory of Solids :

The atoms have energy levels similar to the energy states of all atoms. On the basis of energy bands solids can be classified into conductor, insulator and semiconductor.

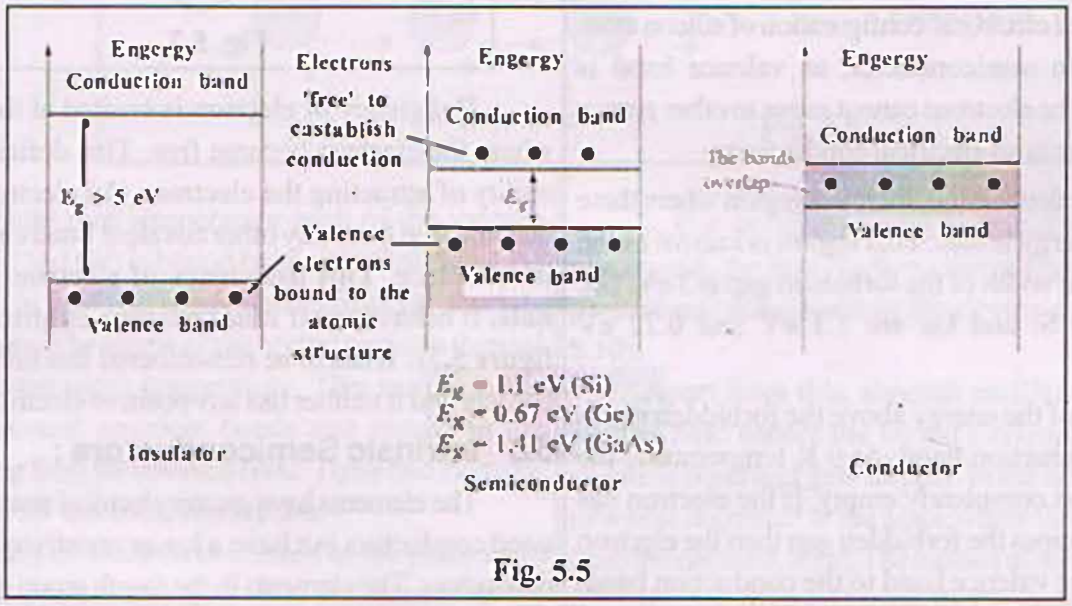


Fig. 5.5

Conductors :

Figure 5.6 shows the band structureof a sodium atom, which explains the reason why it is a good conductor of electricity. The electronic configuration of sodium atom is given as $1s^2\ 2s^2\ 2p^6\ 3s^1$. There are 2 N valence states for the 3s state. Out of which N states are filled due to the contribution of one electron from each of the sodium atom. The remaining N states are empty. As a result, the electrons can move easily into the empty available states and contribute

towards electrical conductivity. In many of the metals, the conduction and the valence bands overlap each other. In such a situation too the electrons contribute in the electrical conduction.

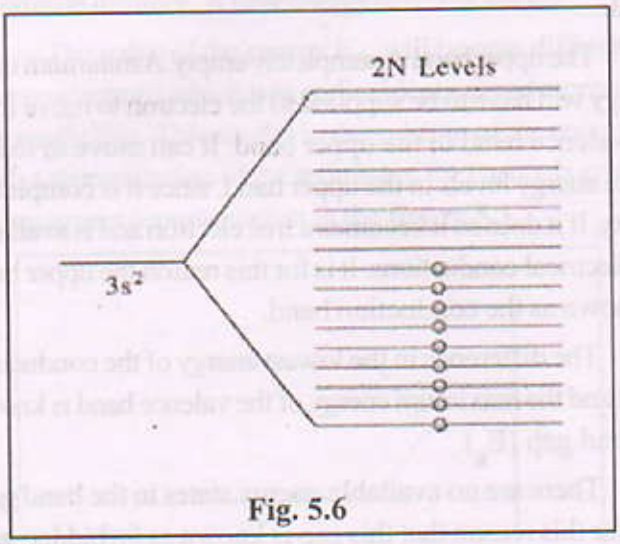


Fig. 5.6

Insulators :

In substance where the forbidden gap between the valence band and the conduction band is very large (>3eV), the electrons can not move easily from the valence band to the conduction band. Therefore, such a substance does not conduct electricity.

Semiconductors :

We discussed electronic configuration of silicon atom in above topic. In semiconductor, as valence band is completely filled, the electrons cannot move to other energy levels. Hence, there is no electrical conductivity.

Above the valence band, there is a region where there is no available energy levels. This region is known as the forbidden gap. The width of the forbidden gap is 3 eV. The values of E_g for Si and Ge are 1.1 eV and 0.72 eV respectively.

The region of the energy above the forbidden gap is known as the conduction band. At 0 K temperature, the conduction band is completely empty. If the electron has enough energy to cross the forbidden gap then the electron can move from the valence band to the conduction band. These electrons will then contribute towards the electrical conduction.

A hole is created when an electron moves from valence band to the conduction band. The number of holes created is equal to the number of electrons present in the conduction band. Hence in an intrinsic semiconductor number of electrons and holes are same.

- **Concept of Hole :**

At absolute zero temperature each of the valence electrons of Si (and Ge) is bound by the covalent bond. As a consequence Si (and Ge) behave as insulators at absolute zero temperature. The atoms of the crystal perform thermal oscillations at the room temperature. This results in the breaking of several covalent bonds and results in the electrons freeing from the covalent bond. These free electrons are responsible for electrical conduction.

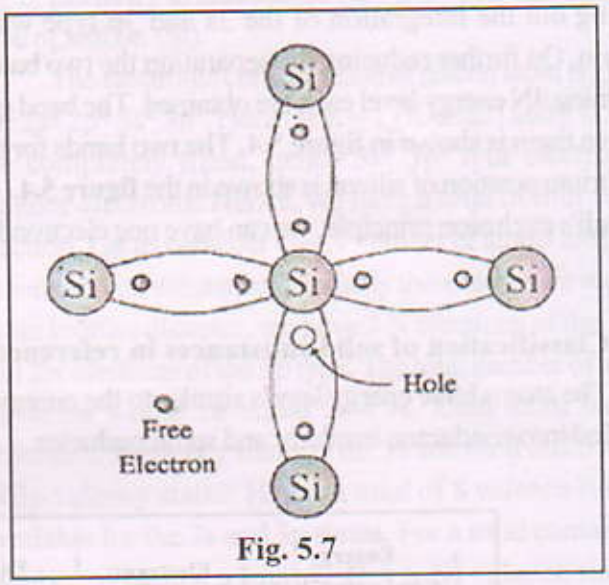


Fig. 5.7

Deficiency of electron is created at the place from where the electron became free. This deficiency has the ability of attracting the electrons. An electron which has become free from any other covalent bond can get trapped in this place. **This deficiency of electron is known as hole.** It behaves as if it has positive electric charge. **(see figure 5.7).** It has to be remembered that hole is not a real particle and it neither has any positive electric charge.

5.3 Intrinsic Semiconductors :

The elements have greater electrical resistivity than the good conductors but have a lower resistivity than the bad conductors. The elements in the fourth group of the periodic table like the Si and Ge have such properties. They are known as semiconductors. We will study here semiconductors Si .

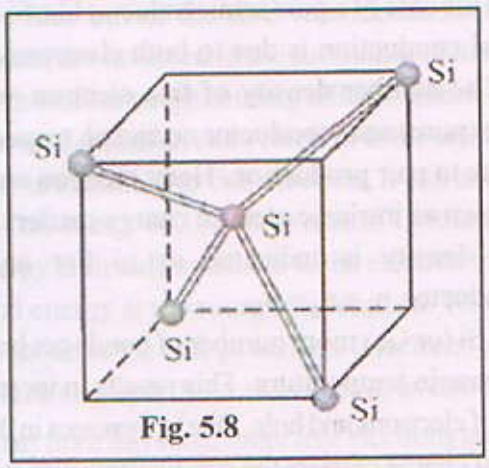


Fig. 5.8

Atomic number of Si is 14. The electronic configuration of Si is $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$. The electrons up to $1s^2\ 2s^2\ 2p^6$ completely occupy the K and L shells. $3s^2\ 3p^2$ electrons are the valence electrons. Hence Si (z = 14) and Ge (z = 32) is tetravalent. Here the two $3s^2$ orbital and two$2p^2$ orbitals combine to form four (sp^3) complex orbitals. These orbitals combine with similar such orbitals of the neighbouring atoms and constitute covalent bond. There are two electrons for every covalent bond. In this way the four valance electrons of the Silicon makes a covalent bond with its four neighbouring atoms by sharing one-one electron. **Figures 5.8 and 5.9** shows the above situation in two dimensions and three dimensions respectively. A crystal lattice of a diamond is obtained if one extends the above arrangement of atoms in three dimensional space. Thus Si and Ge have diamond structure.

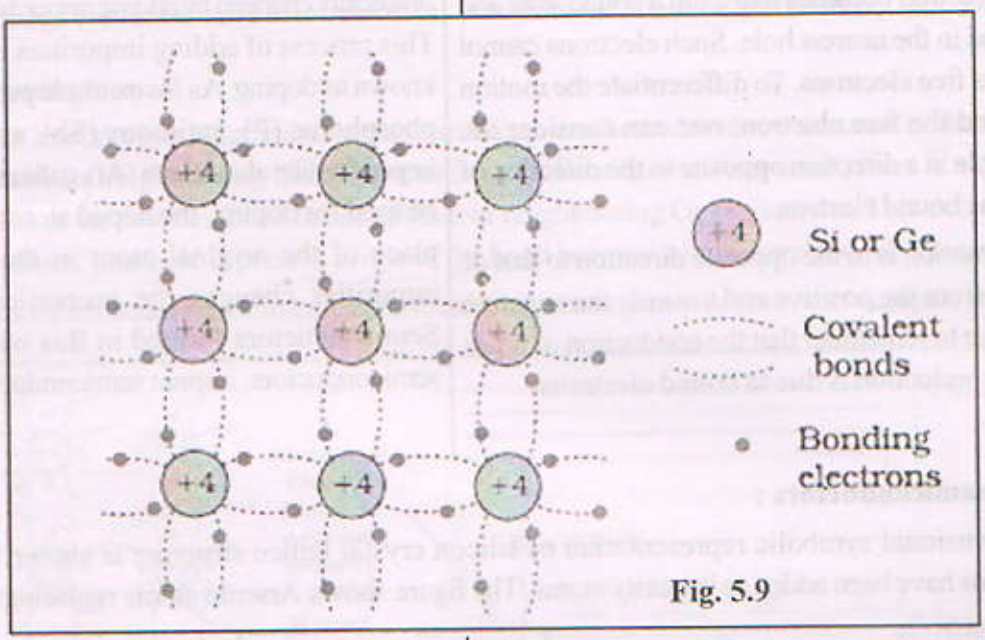


Fig. 5.9

At absolute zero temperature each of the valence electrons of Si (and Ge) is bound by the covalent bond. As a consequence Si (and Ge) behave as insulators at absolute zero temperature. The atoms of the crystal perform thermal oscillations at the room temperature. This results in the breaking of several covalent bonds and results in the electrons freeing from the covalent bond. These free electrons are responsible for electrical conduction.

Deficiency of electron is created at the place from where the electron became free. This deficiency has the ability of attracting the electrons.

An electron which has become free from any other covalent bond can get trapped in this place.

In this situation on applying a p.d. between two ends of a crystal, the free electrons move from negative end to positive end and constitute the electric current **(see figure 5.10).**

Apart from this, thermal oscillations and external electric field causes the bound electrons to be free from covalent bond and gets trapped in the nearest hole. And a new hole is created at the place where the electron escaped from the covalent bond. The motion of the bound electron is from the negative end towards the positive. Hence, it is understood that motion of hole is from positive end towards the negative end.

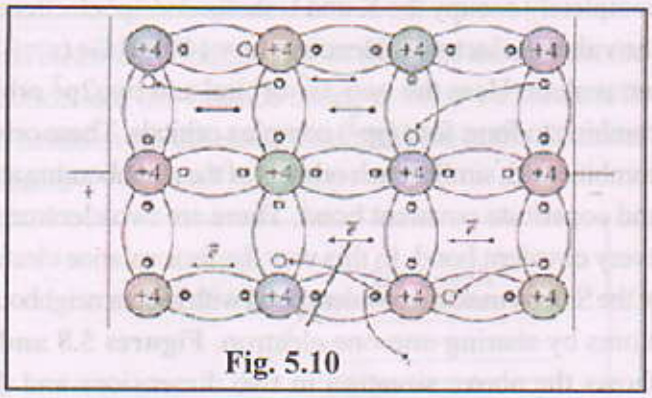


Fig. 5.10

Thus, we get two types of currents in a semiconductor :

(1) Due to motion of free electron (Ie)

(2) Due to motion of bound electron or hole (Ih).

Such an electron becomes free from a bound state and again gets bound in the nearest hole. Such electrons cannot be considered as free electrons. To differentiate the motion of the bound and the free electron, one can consider the motion of the hole in a direction opposite to the direction of the motion of the bound electron.

Since its motion is in the opposite direction to that of the electron i.e. from the positive end towards the negative end. We will have to remember that the conduction of holes means that the conduction is due to bound electrons.

In the case of a pure semiconductor like Si and Ge, electrical conduction is due to both electrons as well as holes. The number density of free electron and hole in intrinsic (pure) semiconductor ne and nh respectively are equal due to pair production. Here, electron and hole are also known as intrinsic electric charge carriers, hence its number density is indicated as ni For an intrinsic semiconductor, $n_i = n_e = n_h$.

In Si (or Ge) more number of bonds get broken with the increase in temperature. This results in increase in the number of electrons and hole. Due to increases in the number density of charge carriers the conductivity also increases.

5.4 Extrinsic Semiconductors :

The conductivity of the intrinsic semiconductor can be drastically changed by adding impurities in the right proportion. This process of adding impurities in the semiconductor is known as doping. As for example pentavalent impurities like phosphorus (P), antimony (Sb), arsenic (As) or trivalent impurities like aluminium (Al), gallium (Ga) or indium (In) can be used for doping, the doped atoms arrange themselves in place of the original atom in the host crystal. Adding impurities changes the properties of semiconductors. Semiconductors formed in this way are called extrinsic semiconductors, impure semiconductors.

5.4.1 N - type semiconductors :

Two dimensional symbolic representation of silicon crystal lattice structure is shown in **figure 5.11.** Here the Arsenic atoms have been added as impurity atoms. The figure shows Arsenic atoms replacing one silicon atom.

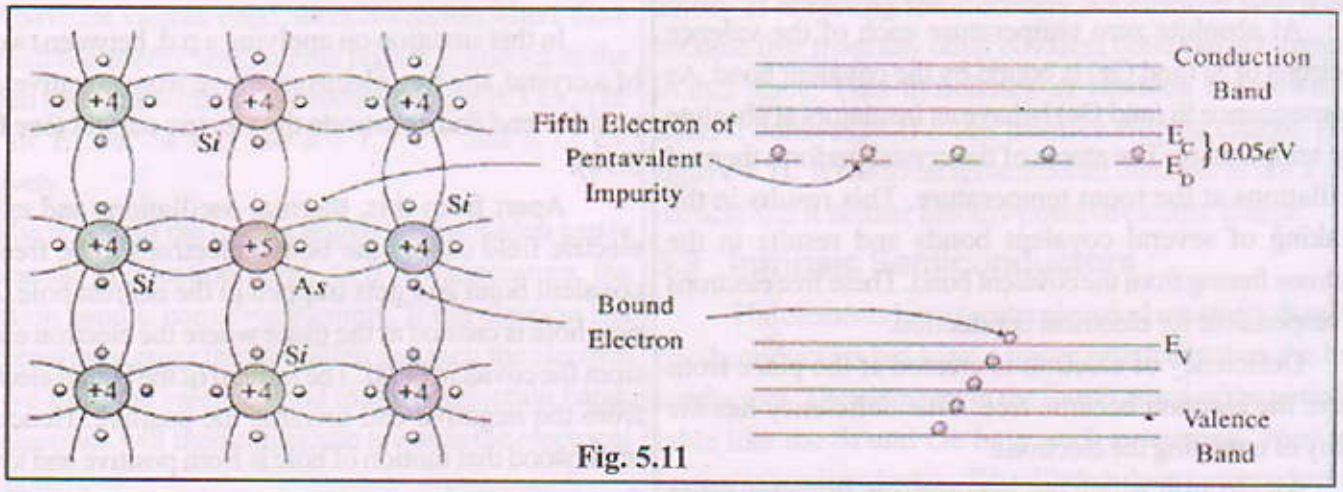


Fig. 5.11

The four out of the five valence electrons of the Arsenic atom are involved in the formation of the covalent bonds with its four neighbouring silicon atoms. The fifth electron is available as an extra electron to the crystal. If 0.05 eV energy is available to this electron, it can act as a free electron. This energy is 0.01 eV in case of Germanium. This much energy is already available to the electron in the form of thermal energy at the room temperature. The impurity atoms donate electric charge carriers (electron) to the host crystal. Such an impurity atom is known as donor atom.

Apart from this some more free electrons are obtained due to the breaking of the bonds resulting in the formation of the holes. Their number is very small compared to the number of free electrons donated by the impurity atoms. We can thus say that the charge carriers available for electrical conduction is primarily obtained from the electrons donated by the impurity atoms. Thus electrons are known as majority charge carriers, in the case of the addition of pentavalent impurities. The electron carries negative charges and hence such a crystal is known as N-type semiconductor crystal, deriving its name from the first letter of the word Negative. The electrical conduction due to holes in such a crystal is very less, so holes are known as minority charge carriers. It is very clear that $n_e > n_h$.

Their proportion is kept as approximately as 1 in 10^6 pure atoms. Hence, 1 mole crystal contains approximately 10^{17} impure atoms. Each of these impurity atoms contribute one electron. 1 mole crystal contains approximately 10^{17} free electrons. A metal like copper which is a good conductor contains approximately 10^{23} free electron.

5.4.2 P - type semiconductors :

If we add trivalent impurity like Aluminium in the Germanium or silicon then three electrons of these impurity atoms form covalent bonds with its neighbouring three Germanium or Silicon atoms. As a result, there is a deficiency of one electron in the formation of the covalent bond in one of the four neighbouring Ge or Si atoms. This deficiency of electron can be considered as a hole. This hole is present in one of the bond between aluminium and silicon atom.

This hole attracts electron and hence in this sense the aluminium impurity is known as acceptor impurities.

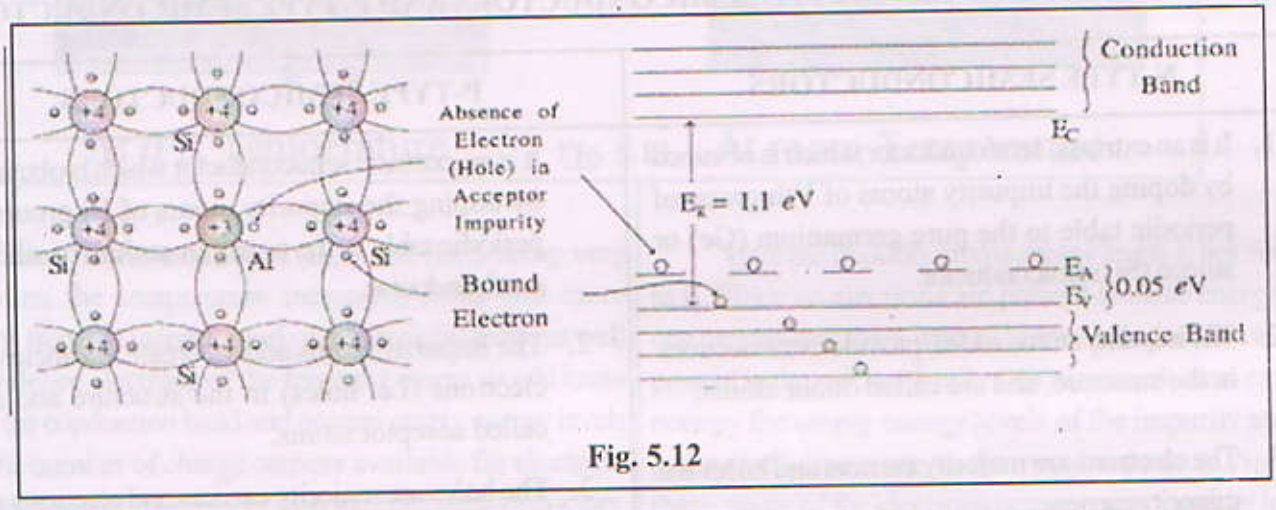


Fig. 5.12

The electrical conduction in such a crystal is primarily due to holes.

Figure 5.12 shows symbolic representation of Aluminium impurity added to a Germanium.

Holes behave as a positively charged particle. Hence, such a semiconductor is known as P-type semiconductor. Holes are the majority carriers while electrons are the minority charge carriers in a P-type semiconductor.

In this case $n_h > n_e$.

• DISTINCTION BETWEEN INTRINSIC AND EXTRINSIC SEMICONDUCTORS :

INTRINSIC SEMICONDUCTOR	EXTRINSIC SEMICONDUCTOR
1. It is pure semiconducting material and no impurity atoms are added to it.	1. It is prepared by doping a small quantity of impurity atoms to the pure semiconducting material.
2. Examples are crystalline forms of pure silicon and germanium.	2. Examples are silicon and germanium crystals with impurity atoms of arsenic, antimony, phosphorous etc. or indium, boron, aluminium etc.
3. The number of free electrons in conduction band and the number of holes in valence band is exactly equal and very small indeed.	3. The number of free electrons and holes is never equal. There is excess of electrons in n-type semiconductors and excess of holes in p-type semiconductors.
4. Its electrical conductivity is low.	4. Its electrical conductivity is high.
5. Its electrical conductivity is a function of temperature alone.	5. Its electrical conductivity depends upon the temperature as well as on the quantity of impurity atoms doped in the structure.

• DISTINCTION BETWEEN N-TYPE SEMICONDUCTORS AND P-TYPE SEMICONDUCTORS

N-TYPE SEMICONDUCTORS	P-TYPE SEMICONDUCTORS
1. It is an extrinsic semiconductor which is obtained by doping the impurity atoms of Vth group of periodic table to the pure germanium (Ge) or silicon (Si) semiconductor.	1. It is an extrinsic semiconductor which is obtained by doping the impurity atoms of III group of periodic table to the pure germanium or silicon semiconductor.
2. The impurity atoms added, provide extra electrons in the structure, and are called donor atoms.	2. The impurity atoms added, create vacancies of electrons (i.e. holes) in the structure and are called acceptor atoms.
3. The electrons are majority carriers and holes are minority carriers.	3. The holes are majority carriers and electrons are minority carriers.
4. The electron density (n_e) is much greater than the hole density (n_h) i.e. $n_e >> n_h$	4. The hole density (n_h)is much greater than the electron density (n_e) i.e. (n_h) >> (n_e)
5. The donor energy level is close to the conduction band and far away from valence band.	5. The acceptor energy level is close to valence band and is far away from conduction band.

5.4.3 Electrical conduction in N type semiconductors :

Figure 5.13 shoves the energy levels in N-type semiconductors which helps in understanding the electrical conductivity in N-type semiconductor. The figure shows the completely filled valence band (Ev) as well as the completely empty conduction band (Ec). Apart from these energy levels the valence energy levels of the impurity atoms (ED Donor) is also indicated by the dashed lines. The above situation refers to 0 K temperature.

At 0 K temperature one electron each of the impurity atom occupies one of these energy levels. We are aware of the fact that the impurity atoms are scattered in the crystal structure of the semiconductor. The wave function of these valence states lie closer to the impurity atoms or in other words are not present in the entire crystal. Hence the symbolic representation is shown by dotted line.

ED and Ecare very near. For Silicon (Si) the difference between ED and Ec is 0.05 eV and for germanium (Ge) the difference between ED and Ec is 0.01 eV.

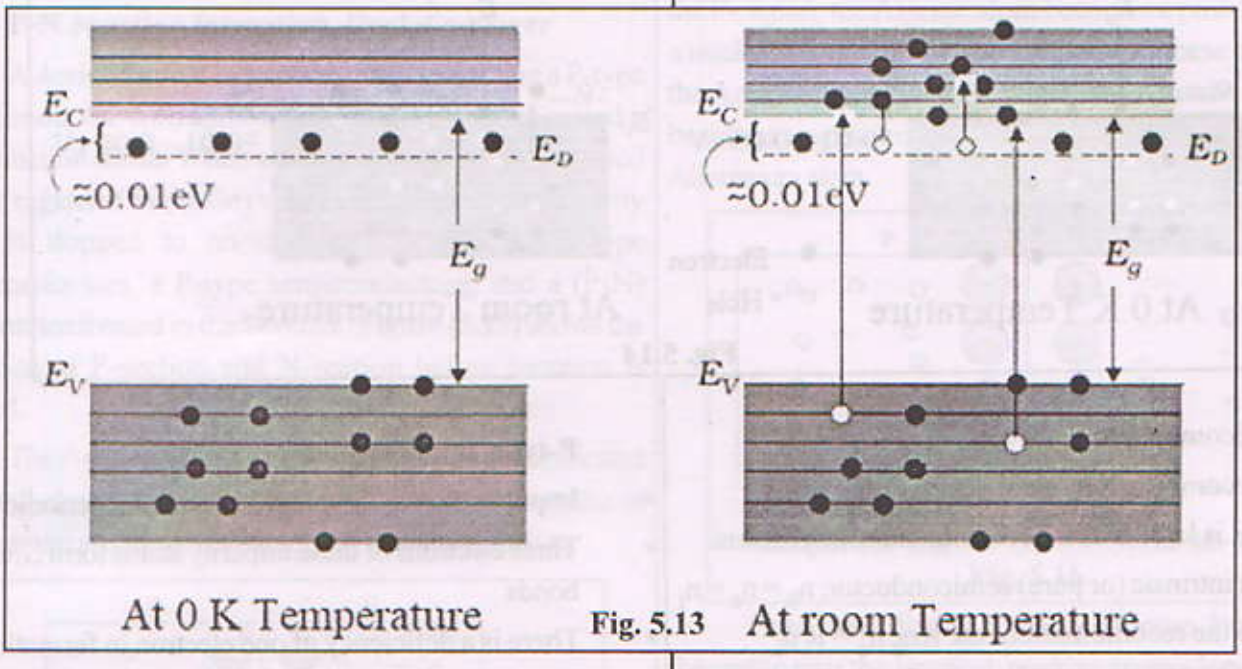


Fig. 5.13

The difference between (ED) and (EC) being very less, when the temperature increases, more and more electrons from the valence band of the semiconductor as well as the valence electrons of the impurity atoms would cross over to the conduction band and occupy empty energy levels in it. The number of charge carriers available for electrical conduction will be much more than the pure semiconductors. Hence, in N-type semiconductor $n_e > n_h$.

5.4.4 Electrical conduction in P type semiconductors :

Figure 5.14 shows the energy levels of the P-Type semiconductor.

It shows the completely filled valence band (Ev), the valence energy levels of the impurity atoms (E_A Acceptor) as well as the completely empty conduction band (Ec). The above situation is at 0 K temperature.

Here the impurity atoms energy levels E lies very close to E. Since no electrons are present at these energy levels one can say that there is an existence of holes. The electrons present in the valence band of the semiconductors can easily occupy the empty energy levels of the impurity atoms on getting sufficient energy at the room temperature. Apart from these, some of the electrons occupy empty energy levels in the conduction band and as a result create holes in large numbers and the possibility of the motion of the electrons also increases.

Hence in P-type semiconductor the number of charge carriers (Holes) available for electrical conduction will be much more than the pure (Intrinsic) semiconductors. Hence, in P-type semiconductor $n_h > n_e$.

Hence in a P-type semiconductor the electrical conductivity is much more than the electrical conductivity of a pure semi conductor.

The creation of electron hole pair due to the migration of the electron to the conduction band is not a very stable situation. The electrons and holes collide with each other as per the laws of thermodynamics and the temperature. The electrons once again occupy the hole, the creation of the electron hole pair and its recombination process takes place at the same time. In the equilibrium position the rate of electron hole pair formation and their recombination is equal.

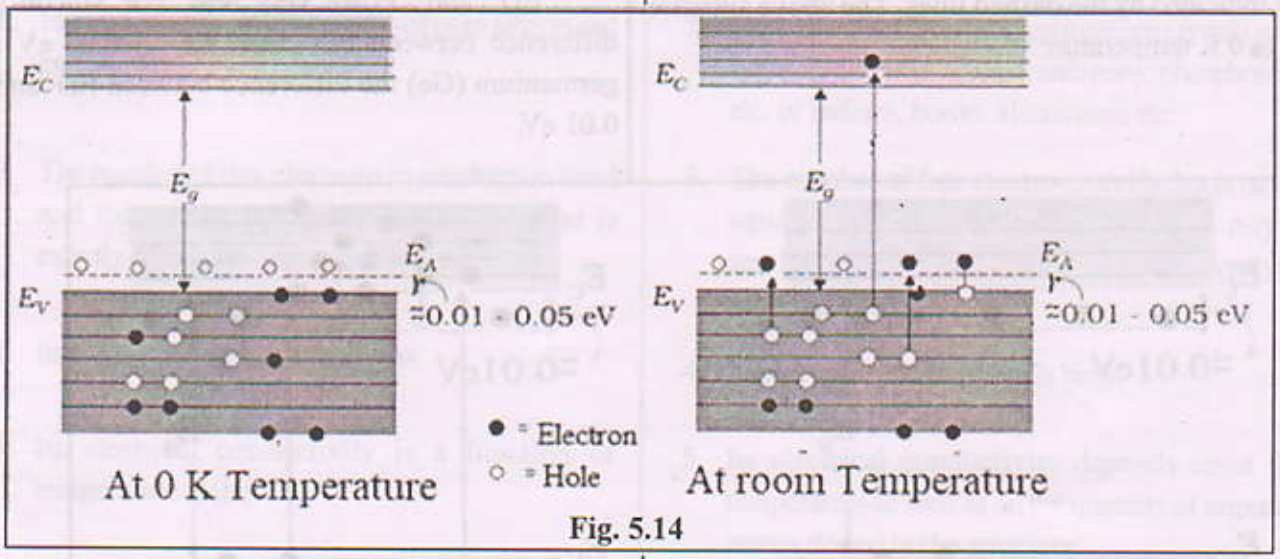


Fig. 5.14

The recombination rate $\propto n_h n_e$

The recombination rate = $Rn_h n_e$

Here R is known as the recombination coefficient.

For an intrinsic (or pure) semiconductor, $n_h = n_e = n_i$

Hence the recombination rate $Rn_h n_e = R n_i^2$

The recombination rate for an intrinsic semiconductor and its extrinsic semiconductor are equal.

$R n_i^2 = Rn_h n_e$

$n_i^2 = n_h n_e$

Let us remember N type and P type semiconductors.

N-type semiconductor :

- impurity atoms - Pentavelent , Vth group of periodic table
- The four out of the five valence electrons are involved in the formation of the covalent bonds and fifth electron is available as a free electron
- One free electron is obtained from each impurity atoms
- The impurity atoms are called donor atoms
- The electrons are majority carriers
- $(n_e) >> (n_h)$

P-type semiconductor :

- Impurity atoms- Trivelent , III group of periodic table
- Three electrons of these impurity atoms form covalent bonds
- There is a deficiency of one electron in formation of the covalent bond in one of the four neighbouring atoms. This deficiency of electron is called a hole.
- The impurity atoms are called Acceptor atoms.
- The holes are majority carriers.
- $(n_h) >> (n_e)$

5.4.5 Temperature Dependence of Conductivity for a Semiconductor :

With increase in temperature, more covalent bonds are broken and hence more electrons and holes are produced as charge carriers. And hence electrical conductivity of semiconductor increases with increase in temperature.

5.5 P-N Junction diode :

A P-N junction is the basic building block of many semiconductor devices like diodes, transistor, etc. A clear understanding of the junction behaviour is important to analyse the working of other semiconductor devices. We will

now try to understand how a junction is formed and how the Junction behaves under the influence of external applied voltage (External applied voltage is called bias).

Semiconductors, like Germanium (Ge) and Silicon (Si) are called intrinsic (elemental) semiconductors. P–N junction diode, zener diode, transistor etc. are fabricated from it. Apart from these elemental semiconductors, non carbonic semiconductors like CdS, GaAs, CdSe etc., some organic compounds as well as polymer organic materials are also included in semiconductors. Solar Cells, LEDs, Laser Diodes are made from non carbonic semiconductors.

5.5.1 P-N Junction formation, Depletion layer

A device formed by permanently connecting a P-type semiconductor with an N-type semiconductor is called a P-N junction diode. When a donor impurity (As) is dopped to one region of Si (or Ge) wafer and an acceptor impurity (AI) is dopped to another region then an N-type semiconductors, a P-type semiconductors, and a (P-N) junction are formed in the Si wafer. **Figure (5.15)** shows the situation of P-section and N-section before junction is formed.

The P-region contains higher number of holes, indicated by small circles. In the figure, 4 acceptor impurity atoms of Aluminium are shown in the region near the junction.

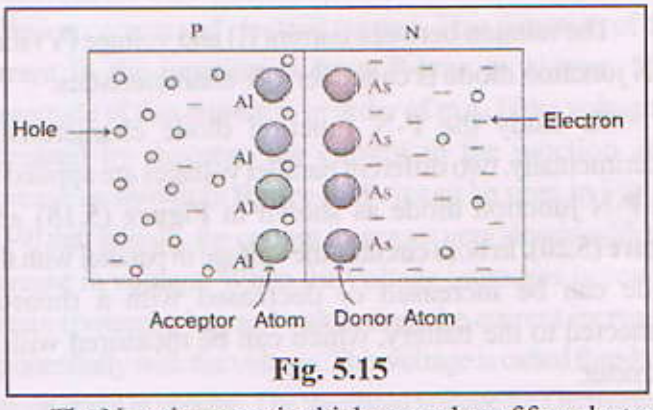


Fig. 5.15

The N-region contains higher number of free electrons, indicated by a small line (-). In figure, 4 donor impurities of arsenic are shown in the region near the junction. In this situation both P-region and N-region are electrically neutral.

Now, let's take an example to understand how diffusion of electrons and holes takes place. If a porous rubber membrane like partition is placed between the high-density and low-density gases in a gas vessel, the gas molecules move from the high-density region to the low-density region through the porous membrane.

Here, since the number of free electrons in the N-region is much more than the number of free electrons in the P-region, the electrons in the N-region diffuse to the P-region through the P-N junction, i.e. the electrons enter from the N-region to the P-region through the junction and fill the holes in the P-region near the junction. In addition, there is also a very small diffusion of holes from P-region to N-region

Figure (5.16) shows the situation after some diffusion. The 4 electrons from the 4 Arsenic atoms in the N-region are shown to defuse into the holes of the 4 Aluminium atoms in the P-region. As the electrons of the Arsenic atom move to the P-region, the Arsenic atom becomes a positive ion with a nuclear charge of +1. And similarly, as these electrons on the Arsenic atom enter the hole in the Aluminium band, it becomes a negative ion with a nuclear charge of –1 on the Aluminium atom.

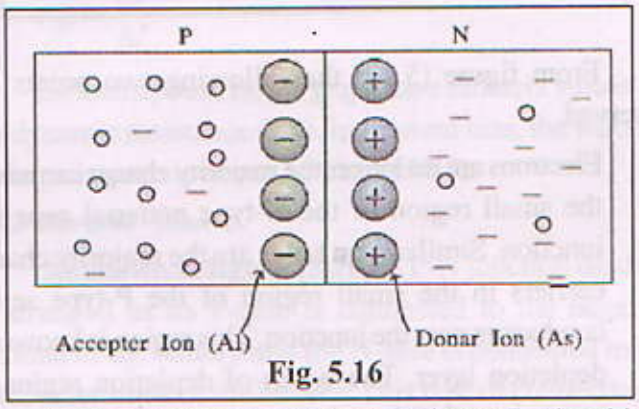


Fig. 5.16

Thus, the diffusion process continues. During this, in the region near the junction, positive arsenic ions increase in the N-region, i.e., positive charge gets accumulated in the N-region and the negative aluminium ions increase in the P-region. i.e., negative charge gets accumulated in the P-region. These charges are steady as they are the charges on the ions.

Thus, a positive potential is established in the N-region and a negative potential is established in the P-region. Note that, the potential at the junction is considered to be zero. In such a situation, when the electron move from the N-region to the P-region, it has to face this electric field. When this electric field becomes strong enough, electron-hole diffusion stops.

Due to this situation, the potential established in the region near the junction is shown in the figure and graph of the state established in the region near the junction is shown in figure and graph **Fig. (5.17).**

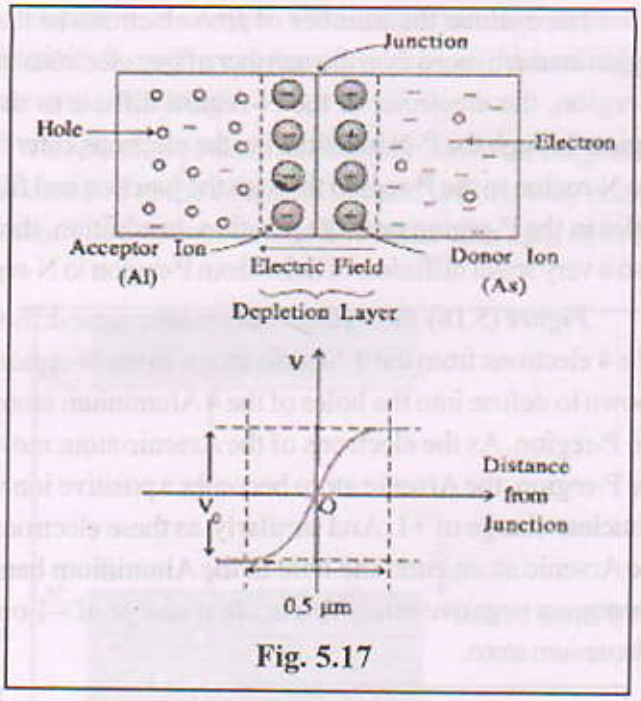


Fig. 5.17

From figure (5.17) the following two points are observed.

(1) Electrons are no longer the majority charge carriers in the small region of the N-type material near the junction. Similarly on holes are the majority charge carriers in the small region of the P-type semiconductors near the junction. This region is known as depletion layer. The width of depletion region is approximately 0.5 μm.

(2) The distribution of electric potential in the depletion layer is called the depletion barrier or potential barrier. This potential barrier is in order of 0.1 V. This value is about 0.7 V for Si and 0.3 V for Ge.

Thus, from the above two points, it can be said that if the charge carrier has to cross the junction to the other region, it has to cross this depletion barrier and it requires energy.

In PN Junction, the magnitude of depletion barrier and width of depletion region are dependent on the concentration of the impurity added to the P and N type semiconductor. The depletion region is wider if the amount of impurity atom added is less and the electric field becomes weaker near the junction. The width of the depletion region decreases with the increase in the impurity concentration. This increases the intensity of electric field near the junction. Thus, the characteristics of the junction can be changed by increasing or decreasing the impurity concentration. As a result we can fabricate different types of the semiconductor devices.

Only for information

Due to the positive and negative charges located in the depletion layer, its properties are similar to those of a capacitor. This capacitance formed near the depletion layer of P-Njunction is called depletion capacitance (Cd) or transition capacitance (Ct).

Increasing the value of the reverse bias voltage in a P – N junction diode, increases the width of the depletion region, resulting in a decrease in the value of the depletion capacitance. ($C \propto 1/d$, where, C = Capacitance, d = Width of depletion region)

Thus, by changing the value of the reverse bias voltage of the P – N junction diode, the value of the (depletion) capacitance can also be changed. Hence it is also called Varactor diode or Variable capacitor diode.

5.6 P – N Junction diode, forward and reverse bias characteristics :

The relation between current (I) and voltage (V) for a P -N junction diode is called its I-V characteristics.

To study the P-N junction diode characteristic experimentally, two different parallel voltages are applied to the P-N junction diode as shown in **Figure (5.18)** and **Figure (5.20).** In both circuits, the voltage in parallel with the diode can be increased or decreased with a rheostat connected to the battery, which can be measured with a voltmeter.

5.6.1 Forward Bias :

As shown in **Fig. (5.18)**, when the positive terminal of battery is connected to P side of junction and negative terminal connected to N side of junction, such a connection is known as **forward bias.**

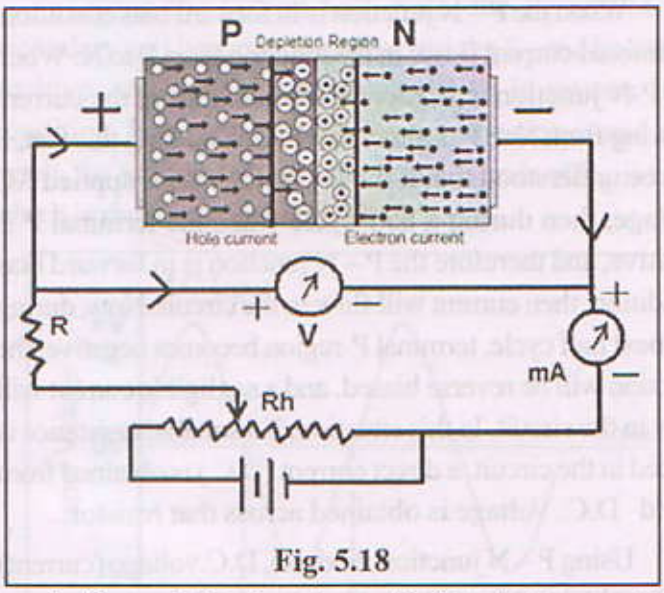


Fig. 5.18

In forward biasing, the emf of the battery and the potential difference across the depletion layer are in opposite direction. Therefore, the width and height of the depletion barrier reduces, so electrons have to do less work to move from N to P. Hence, such a connection is called forward bias. Electrons moves from N-region to P-region under the influence of external battery. Similarly, hole can easily cross the junction from P-type to N-type. Thus, there is a flow of current in the junction due to both types of majority charge carriers. In forward bias the total current is sum of the hole diffusion current and electron current. This direction of the current in the junction is from P-type to N-type. The magnitude of this current is in order of mA. If the voltage is increased by rheostat, the current in the junction also increase as shown in **figure 5.19.** It can be seen in Figure (5.19) that initially the current increases very slowly with the increase in voltage. When the voltage increases beyond a certain (potential barrier) value, then the current increases exponentially with the voltage. This voltage is called threshold voltage or cut in voltage. The threshold voltage for Germanium is ≈ 0.3 V and for Silicon the threshold voltage is ≈ 0.7 V.

Generally, conductors obey Ohm's law and have a linear relationship between current and voltage. Here in this case, the current-voltage relationship is not linear, so in such a case the diode resistance can be found as follows.

The dynamic resistance (rfb) (fb = forward bias) at any point on the characteristics curve in **figure (5.19)** can be found by taking the voltage and current changes near this point as ΔV and ΔI respectively, and taking their ratio.

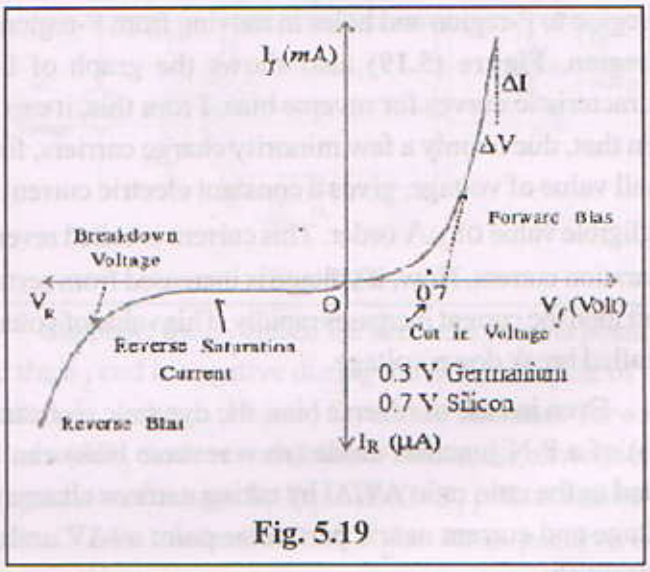


Fig. 5.19

$$r_{fb} = \frac{\Delta v}{\Delta I}$$

Different points on the graph have different values of this dynamic resistance (rfb). In forward bias, the value of diode resistance is about 10 Ω to 100 Ω.

5.6.2 Reverse Bias :

As shown in **figure (5.20)**, a P-N junction diode is so arranged as its P-side is connected to the negative terminal of the battery and the N-side is connected to the positive terminal of the battery. This type of connection is called **Reverse Bias.**

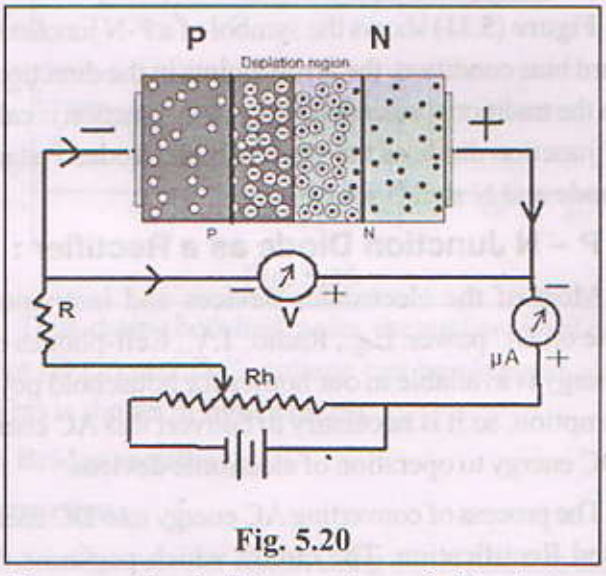


Fig. 5.20

By connecting in this way, the emf of the battery and the potential difference in the depletion layer are mutually helping. Therefore, the width of the depletion layer increases,

so that electrons face more difficulty in moving from N-region to P-region and holes in moving from P-region to N-region. **Figure (5.19)** also shows the graph of I–V characteristic curves for reverse bias. From this, it can be seen that, due to only a few minority charge carriers, for a small value of voltage, gives a constant electric current of negligible value of μA order. This current is called reverse saturation current. Now, if voltage is increased from certain limit then the current increases rapidly. This value of voltage is called break down voltage.

Even in case of reverse bias, the dynamic resistance (rrb) of a P-N junction diode (rb = reverse bias) can be found as the ratio ratio $\Delta V/\Delta I$ by taking a minor change of voltage and current near a particular point as ΔV and ΔI respectively.

$$r_{rb} = \frac{\Delta V}{\Delta I}$$

The reverse bias dynamic resistance (rrb) is very large i.e. of the order of $\sim 10^6\ \Omega$. (Because ΔI is of the order of μA of very small value.)

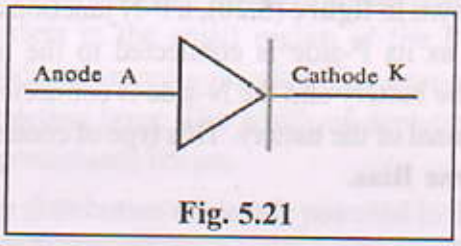


Fig. 5.21

Figure (5.21) shows the symbol of a P-N junction. In forward bias condition, the arrow points in the direction in which the traditional current flows. A P-N junction is called a P-N junction diode as there are two electrodes P stands for anode and N stands for cathode.

5.7 P – N Junction Diode as a Rectifier :

Most of the electronics devices and instruments operate on DC power. E.g., Radio, T.V., Cell-phones etc. AC energy is available in our homes for household power consumption, so it is necessary to convert this AC energy into DC energy to operation of electronic devices.

The process of converting AC energy into DC energy is called Rectification. The circuit which performs this process is called rectifier. A P-N junction diode can be used for the rectification. Hence it is called a P-N junction diode rectifier.

When the P – N junction is in forward bias condition, traditional current flows in the junction from P to N. When the P-N junction is in reverse bias condition, the current flowing from N to P is almost zero. Considering this fact, it can be understood that if the P – N junction is applied AC voltage, then during a half-cycle when the terminal P is positive, and therefore the P – N junction is in forward bias condition, then current will flow in the circuit. Now, during the next half cycle, terminal P-region becomes negative, the junction will be reverse biased, and a negligible current will flow in the circuit. In this situation, if a suitable resistance is placed in the circuit, a direct current (D.C.) is obtained from it and D.C. Voltage is obtained across that resistor.

Using P – N junction diode(s), D.C.voltage (current) can be obtained from the A.C. voltage (current).

5.7.1 Half Wave Rectifier :

Construction :

As shown in **figure 5.22,** the primary coil of the transformer P_1P_2 is connected to A.C. (mains) voltage source. The secondary coil S_1S_2 of the transformer, one end S_1 is connected to the P terminal of the diode and the other end S_2 is connected to the N terminal of the diode through a load-resistance R_L.

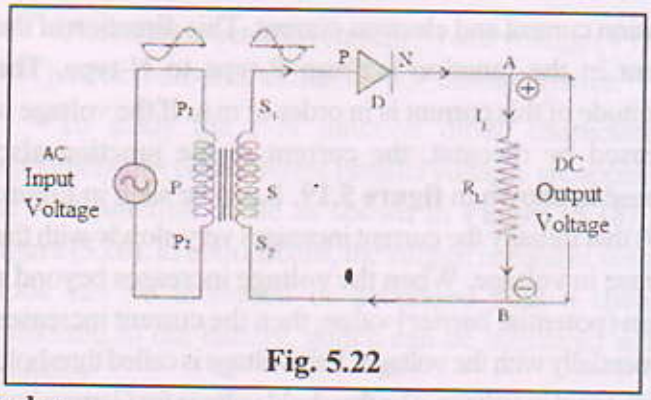


Fig. 5.22

Work :

As shown in **figure (5.22)**, when AC (input) voltage is applied to this electrical circuit, during the first half cycle, S_1 end of the secondary coil is positive with respect to the S_2 end, and as a results the P-N junction in forward bias condition. In such situation the conventional current flows on S_1-P-N-A-B-S_2- S_1 path as shown in **figure (5.22)**. In this condition, current flows from A to B in the load resistance R_L. Thus, this time the A end is positive and the B end is negative. The voltage across AB during this half cycle is called output D.C. voltage, which is shown in **figure (5.23)**.

During the second half cycle, the S_1 end of the secondary coil becomes negative and the S_2 end becomes positive, and the P-N junction will be in reverse bias condition. Hence no current flows in the circuit and as a result, the voltage between the A and B ends of R_L is zero which is shown in **figure (5.23).**

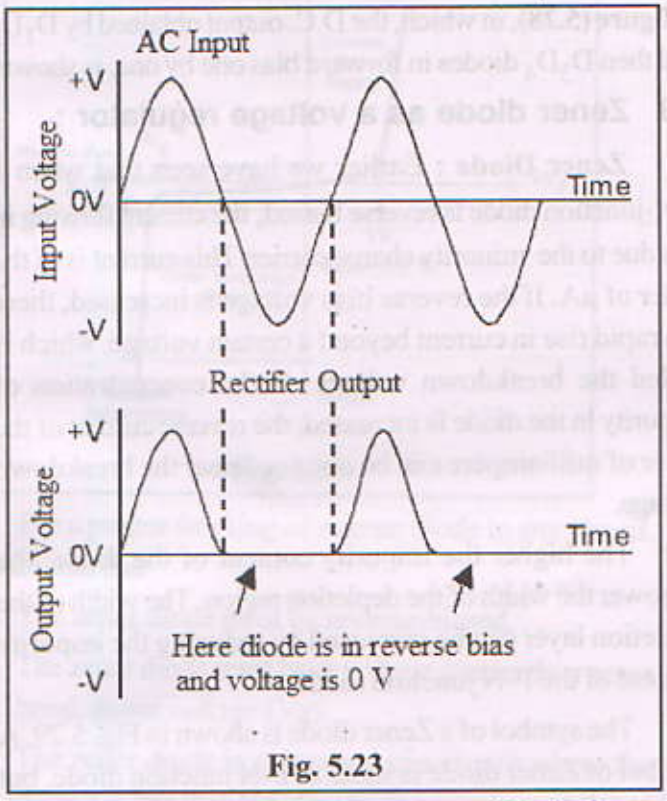


Fig. 5.23

Thus, repeatedly the P-N junction will be in forward and reverse bias condition and a DC voltage is obtained between the two ends of the resistance R_L.

Thus, as we have seen above, in this arrangement we get output across R_L only during the half cycle of the input voltage, it is called a half wave rectifier. This is clearly seen in **figure (5.23).**

5.7.2 Full Wave Rectifier :

Construction :

Figure (5.24) shows the circuit diagram for a full wave rectifier. In this circuit diagram, two P-N junction diodes are used to obtain D.C. voltage across R_L during both half cycles of the complete wave of the A.C. input voltage. In such circuit, a Centre tapped transformer (CT) is used.

Working :

When AC voltage is supplied to this electric circuit as shown in figure (5.24).

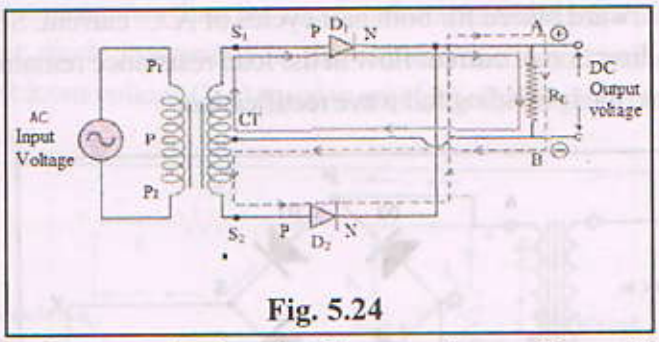


Fig. 5.24

Suppose, the S_1 end of the secondary coil is positive and the S_2 end is negative during the first half cycle of the input A.C. voltage. Hence, D_1 diode becomes forward biased and D_2 diode reverse biased. Hence, the conventional current flows through S_1-D_1-A-B-C- S_1 path as shown in figure (5.24). A-terminal of R_L becomes positive and B-terminal becomes negative.

Now, during the second half cycle of the input A.C. voltage, S_1 end of coil is negative and S_2 is positive. Therefore, D_2 diode becomes forward biased and D_1 diode becomes reverse biased. So, the conventional current flows through S_2-D_2-A-B-C-S_2 path, as shown in figure (5.24). In this half cycle also, A-terminal of R_L is positive, and B-terminal is negative.

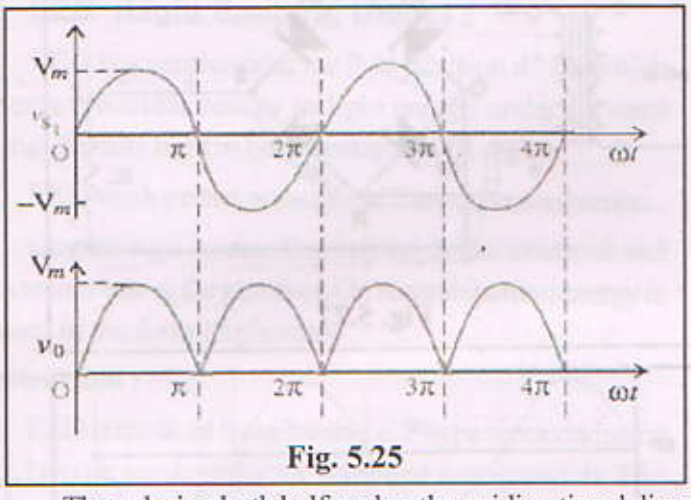


Fig. 5.25

Thus, during both half cycles, the unidirectional direct current (D.C.) and D.C. voltage can be obtained across R_L. This is shown in **figure (5.25).**

5.7.3 Bridge rectifier:

Construction :

A bridge rectifier circuit using 4 P-N junction diodes is used to obtain a full wave rectification. All four P-N junction diodes are connected as shown in **figure (5.26).** In such circuit, any two P-N junction diodes remain

in forward biased for both half cycles of A.C. current. So, the direction of current flow in the load resistance remains same, thus providing full wave rectification.

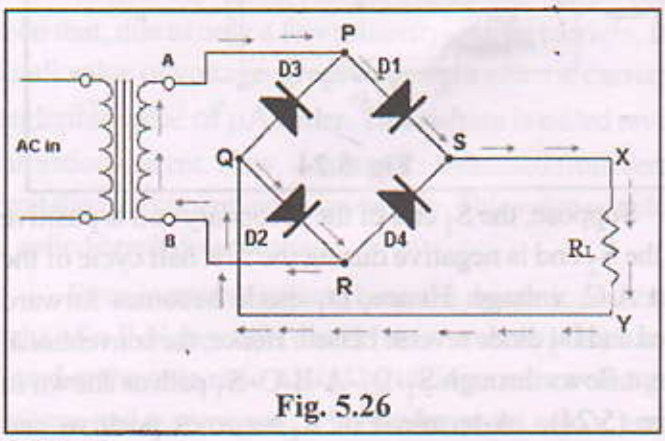


Fig. 5.26

Working :

During the first half cycle of the A.C. current, the P-N junction diodes D_1 and D_2 remain in forward bias as shown in figure (5.26) and current flows along the path A-P- D_1- S-X-Y-Q- D_2 -R-B-A. Meanwhile P-N junction diodes D_3 and D_4 remain in reverse bias.

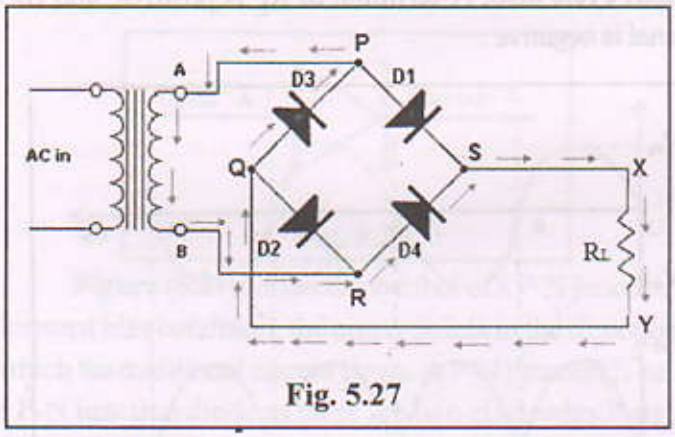


Fig. 5.27

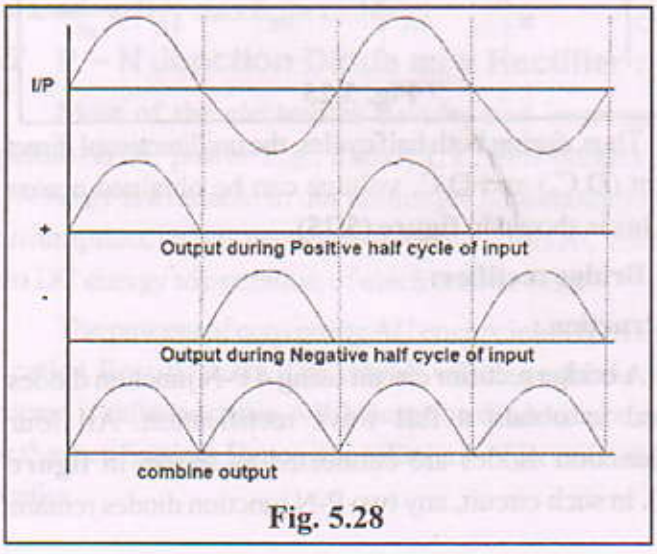


Fig. 5.28

During the second half-cycle of the A.C. current, the P-N junction diodes $D_3$and D_4 remain in forward bias as shown in figure (5.27) and current flows along t A-P-D_3- Q-Y-X-S-D_4- R-B-A path. Meanwhile the P-N junction diodes D_1 and D_2 remain in reverse bias. The A.C. input and the D.C. output obtained from the bridge rectifier is shown in **figure (5.28)**, in which, the D.C. output obtained by D_1D_2 and then D_3D_4 diodes in forward bias one by one, is shown.

5.8 Zener diode as a voltage regulator :

Zener Diode : Earlier we have seen that when a P-N-junction diode is reverse biased, the current flowing in it is due to the minority charge carrier. This current is of the order of μA. If the reverse bias voltage is increased, there is a rapid rise in current beyond a certain voltage, which is called the breakdown voltage. If the concentration of impurity in the diode is increased, the reverse current of the order of milliampere can be obtained near the breakdown voltage.

The higher the impurity content of the diode, the narrower the width of the depletion region. The width of the depletion layer can be increased by reducing the impurity content of the P-N junction diode.

The symbol of a Zener diode is shown in Fig. 5.29. A symbol of Zener diode is same as P-N junction diode, but its cathode line is bent in a 'Z' shape.

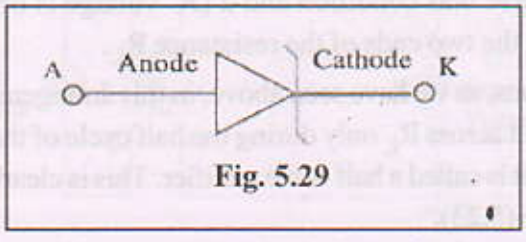


Fig. 5.29

Figure 5.30 shows the characteristic of Zener diode. The forward bias characteristic is similar to that of a conventional P-N junction diode. In reverse bias condition, the value of current is very small (of the order of μA) in the region of low voltage less then breakdown voltage.

Beyond the breakdown voltage (Vz), this current increases suddenly to the order of milliampere , which is called the Zener current (Iz).

Here the breakdown, in case of Zener diode, is very sharp. As can be seen from the reverse bias characteristic graph, a larger change in current can be obtained when a very small change in voltage applied near the breakdown

oltage. In other words, the voltage across the zener diode this condition remains almost constant even for large anges in current. Hence such a diode is used as a voltage gulator circuit.

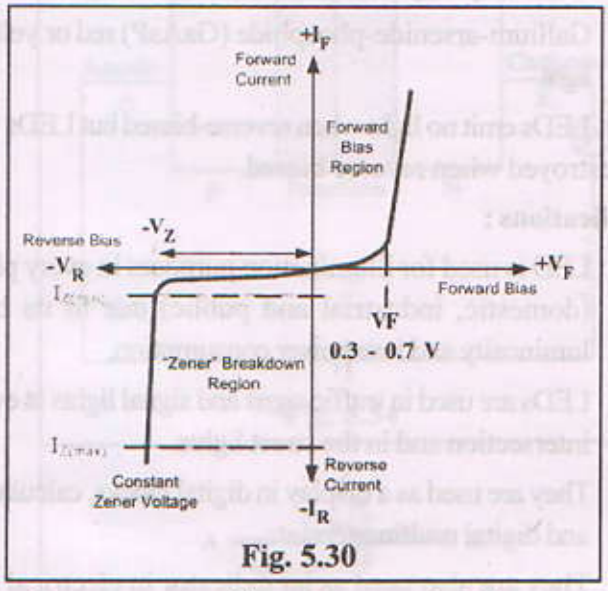


Fig. 5.30

For a proper working of a zener diode in any circuit, is essential that

- The zener diode must be reverse-biased.
- The zener diode must have voltage greater than zener break down voltage **(Vz)**.
- The zener diode is to be used in a circuit where the current is less than the maximum zener current (Iz) of the given zener diode.

ZENER DIODE AS A VOLTAGE REGULATOR :

In a DC power supply made using a rectifier circuit, e change in A.C. mains voltage causes change in the condary coil of the transformer voltage (V_s) . As a result, e D.C. output voltage across the load resistance R_L also anges. Such power supply is called unregulated power pply. A power supply in which the output voltage remains nstant as the input voltage changes, is called a regulated wer-supply. A circuit of a regulated power-supply made ith the help of a Zener diode is shown in Fig. 5.31 .

Zener diode is connected in reverse bias condition as own in the circuit. A resistor (Rs) connected in series with e zener diode, regulates the current. The output voltage is tained across resistance R_L, which is connected parallel to e Zener diode. The input voltage (Vi) applied to the circuit is always greater than the regulated output voltage (Vo). Zener diode connected in the circuit must have zener breakdown voltage (V_z) equal to required regulated output voltage.

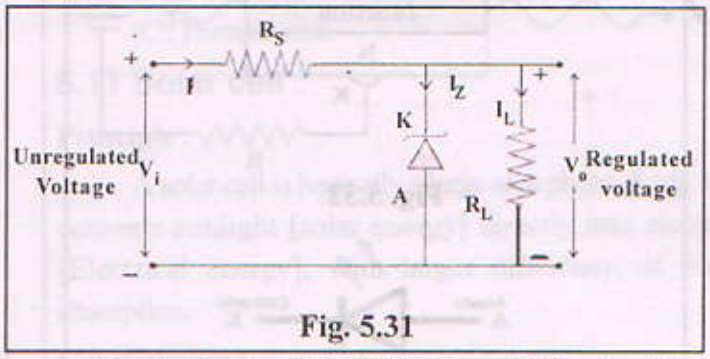


Fig. 5.31

When the input voltage (V_i) ncreases in the circuit, the value of current (I) flowing through (R_s) increases. Hence the voltage drop across R_s increases proportional to the change in input voltage as the voltage across the zener diode (V_z) remains constant. The decrease in the input voltage produces a reverse process. The voltage across drops, which is equal to the drop across the input, and the voltage across the zener remains constant. Thus, the output voltage across the load resistance remains constant. In this way a regulated voltage can be obtained using a zener diode.

5.9 LED (Light Emitting Diode) :

LED is a semiconductor P-N junction diode which converts electrical energy to light energy under forward biasing. It emits light in both visible and IR region.

LED work on the principle of Electroluminescence.

On passing a current through the diode, electrons and holes recombine at the junction. On recombination, energy is released in the form of photons.

Construction :

LED is made of three layers i.e. P-type semiconductor layer, N-type semiconductor layer and active region. The N-layer had the majority of electrons while the P-layer has a majority of holes. The active region has an equal amount of electrons and holes therefore there are no majority charge carriers. The active region is also known as the depletion region. The electrons and holes recombine in this region.

Whenever electron in a Germanium or Silicon atom makes a transition from the conduction band to the valence band then the excess energy of the electron is obtained in the form of heat energy.

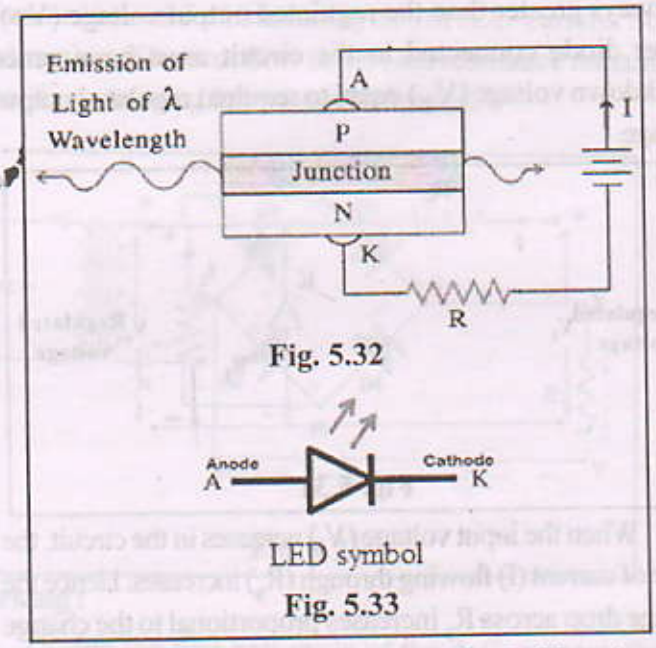


Fig. 5.32

LED symbol

Fig. 5.33

In some of the semiconductors like Gallium Arsenide the energy is obtained in the form of Light. The maximum wavelength of the electromagnetic waves have a wavelength

$$\lambda = \frac{h_c}{E_g}$$

Here, (E_g) is the band gap energy.

h = plank's constant, c = velocity of light in vacuum

In order to effectively obtain the intensity of the light, it is essential that the number of electron in the conduction band and the number of holes in the valence band have to be large. Highly doped N and P type semiconductors are taken and P-N junction is formed.

Working :

The P-N junction diode is kept in fairly large forward bias condition (as shown in Fig. 5.32). Due to large concentration of electron in the N region and large concentration of holes in the P region of the diode, a large current flows through it. The width of the depletion region is extremely small (of the order of few μm) because of large doping in N type and p type. As a result the electrons are easily able to cross the junction and recombine with the holes. On recombination of electron and hole, the energy is emitted in the form of heat and light (i.e., photon). In order to obtain emission in the form of visible light P-Njunction semiconductor diodes are made of materials like gallium arsenide (Ga As), gallium phosphide (GaP) and gallium-arsenide-phosphide (GaAsP) . The colour of light emitted depends upon the type of material used in making the semiconductor diodes as given below :

1. Gallium-arsenide (GaAs) infrared radiation.
2. Gallium-phosphide (GaP) red or green light.
3. Gallium-arsenide-phosphide (GaAsP) red or yellow light.

LEDs emit no light when reverse-biased but LEDs will be destroyed when reverse biased.

Applications :

(1) LED is used for illumination purposes in every place (domestic, industrial and public) due to its high luminosity and low power consumption.

(2) LEDs are used in traffic signs and signal lights at every intersection and in the street lights.

(3) They are used as a display in digital clocks, calculators and digital multimeters, etc.

(4) They are also used as an indicator in electrical and electronic circuits and devices to indicate the supply of power.

(5) It is used in digital camera flashes and torch lights.

(6) LEDs are used in medical equipment.

(7) Laser LEDs that emit light of a single wavelength are used in optical fiber communication.

(8) Colorful LEDs are used for decorations and in toys. LEDs that emit infrared light is not visible to the naked eyes therefore it is used in special applications such as

(9) Infrared LEDs are used in the remote control system in TVs, air conditioners, etc.

(10) In burglar alarm system, it is used to detect the presence of any person passing between them.

5.10 Photo diode :

Principle :

When a P-N junction diode is exposed to light (photons), under reverse bias, it produces electron and hole pairs. Due to the flow of these charge carriers, it produces a reverse current.

Construction :

The construction of photo diode is similar to the normal diode. The only difference between the two is that there is a small window in a photo diode through which the light (Photons) enters and incident on the junction.

This diode is always connected in a reverse bias mode. (see figure 5.34)

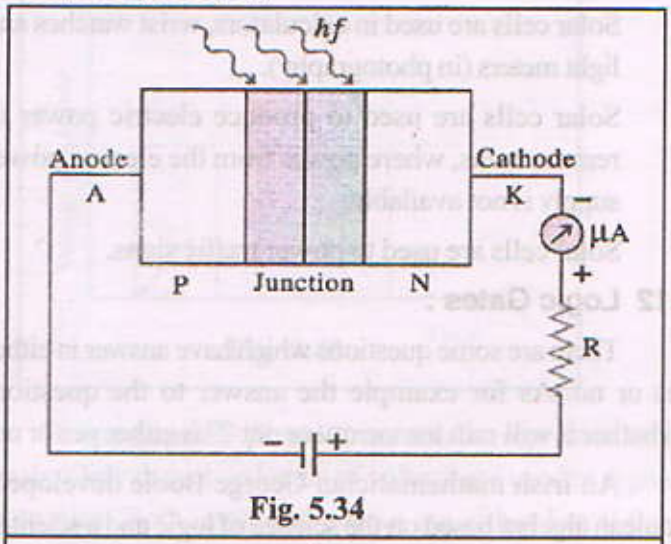


Fig. 5.34

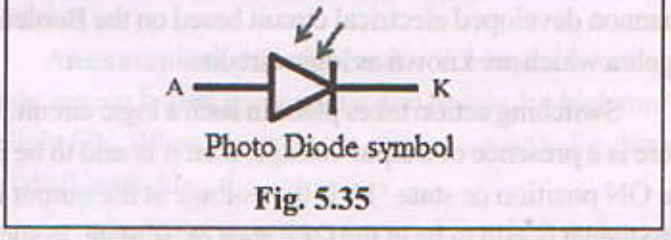


Photo Diode symbol

Fig. 5.35

Working :

When light is made to incident on the P-N junction, and energy of light is $\frac{hc}{\lambda} > E_g$ then each photon creates an electron-hole pair at the junction.

These photo-generated charge carries move towards the potential and therefore constitute a reverse current known as photo current. This reverse current is of the order of μA. The number of electron-hole pair increases on increasing the intensity of light falling on the P-N junction and thus the reverse current increases with the increase in intensity of light.

When no light is incident on the P-N junction of the photo-diode, then no charge carries are created and therefore no current (or) a very little reverse current (IR) flows through the circuit. This current is called Dark current.

Applications :

1. They have wide applications in clocks, camera, street lights, etc.
2. Photo-diodes converts the light into electrical signals. Hence it is widely used in optical communication systems.
3. Photo-diodes are used in electronic devices such as smoke detectors, CD players, TVs, remote controls etc.
4. In medicine they are used in computed tomography (CT) instrument.

5.11 Solar cell :

Principle :

A solar cell is basically a large area photo-diode which converts sunlight [solar energy] directly into electricity [Electrical energy], with larger efficiency, of photon absorption.

Construction :

A solar cell consists of a silicon or gallium-arsenide P-N junction diode with glass window on top. The upper layer is of p-type semiconductor. It is very thin so that the incident light photons may easily reach the P-N junction. The metal lead connected with the N-section of the P-N junction is called the cathode and the metal lead connected with the P-section of the P-N junction is the anode. Which is made in the shape of finger so that anode is not covered by it and the light reach the P-N junction through p-layer as shown in the **figure 5.36.**

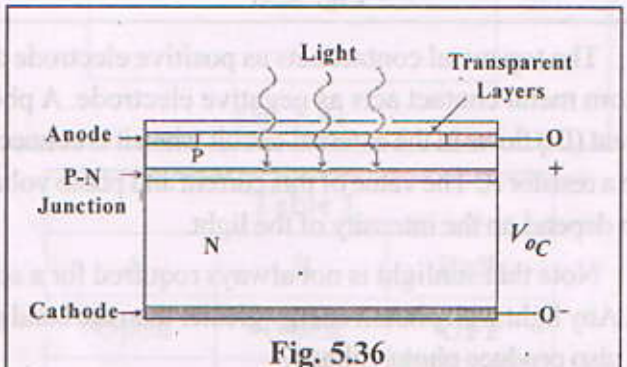


Fig. 5.36

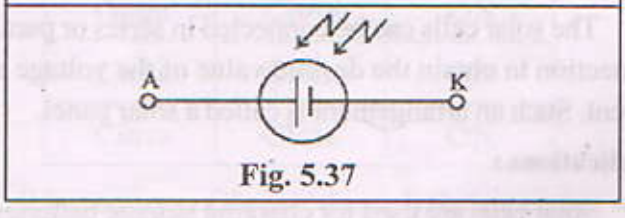


Fig. 5.37

The thin layer of P-type semiconductor is called the emitter and the N-type semiconductor is known as the base. The incident light is directly incident on the P-N junction since the P type material is made up of a very thin layer. The region of the P-N junction is kept large in order to obtain large amount of power.

Working :

When photons of light (of energy hv > E) fall at the junction, electron-hole pairs are generated in the depletion layer (or near the junction). The electrons and holes produced move in opposite directions due to junction field. The photo generated electrons move towards n-side of P-N junction. The photo generated holes move towards p-side of P-N junction. They will be collected at the two sides of the junction, giving rise to emf between the top and bottom metal electrodes. The value of emf is of the order of 0.5 V to 0.6 V.

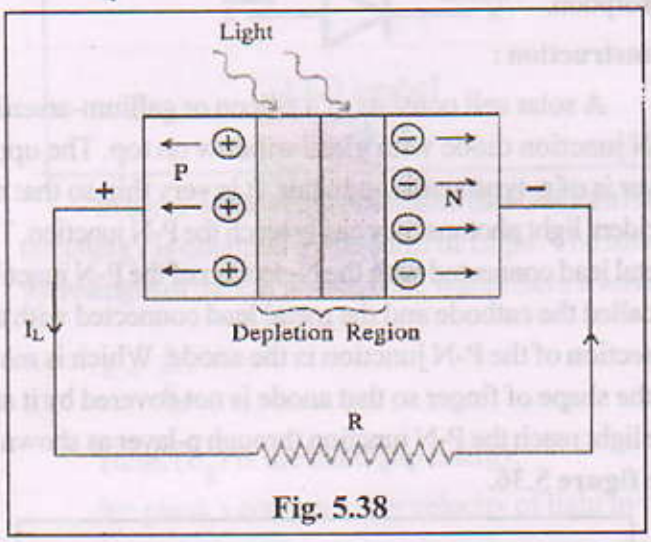


Fig. 5.38

The top metal contact acts as positive electrode and bottom metal contact acts as negative electrode. A photo current (IL) flows in the external circuit when it is connected with a resistor R. The value of this current and photo voltage both depend on the intensity of the light.

Note that sunlight is not always required for a solar cell. Any light with photon energy greater than the band gap will also produce photo voltage.

The solar cells can be connected in series or parallel connection to obtain the desired value of the voltage and current. Such an arrangement is called a solar panel.

Applications :

1. Solar cells are used for charging storage batteries in day time, which can supply the power during night times.
2. The solar cells are also used in artificial satellite to operate the various electrical instruments kept inside the satellite.
3. They are used for generating electrical energy in cooking food and pumping water.
4. Solar cells are used in calculators, wrist watches and light meters (in photography).
5. Solar cells are used to produce electric power in remote areas, where power from the electric power supply is not available.
6. Solar cells are used to power traffic signs.

5.12 Logic Gates :

There are some questions which have answer in either yes or no. As for example the answer to the question "whether it will rain tomorrow or not ?" is either yes or no.

An Irish mathematician George Boole developed Boolean algebra based on the science of logic and a scientist Shannon developed electrical circuit based on the Boolean algebra which are known as logic circuits.

Switching action takes place in such a logic circuit. If there is a presence of output voltage, then it is said to be in the ON position or state '1'. If the voltage at the output is zero then it is said to be in the OFF state or '0' state. In such a circuit the output voltage has only two states hence such a circuit used the binary number system.

If you look at amplifiers or oscillators, the input signal used is a continuous, time-varying current or voltage. These signals can take any value between the minimum and the maximum value of voltage or current. These signals are Continuous or Analogue Signals. They look like as shown in **Fig. 5.39.** These signals are called Analog signals.

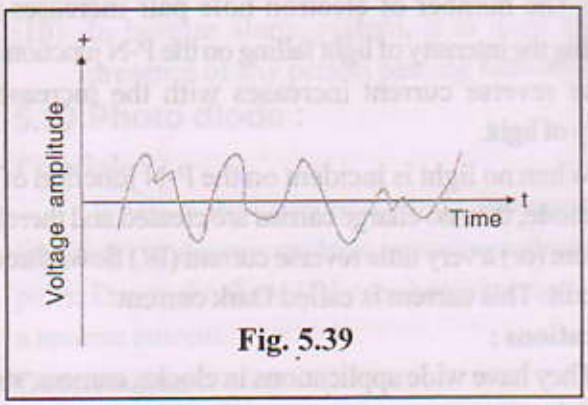


Fig. 5.39

Now, it is possible to have an input signal with discrete values of voltage. Or in simple words, an input signal which provides Level 0 or Level 1 voltage. These signals are Digital Signals; refer to the diagram below:

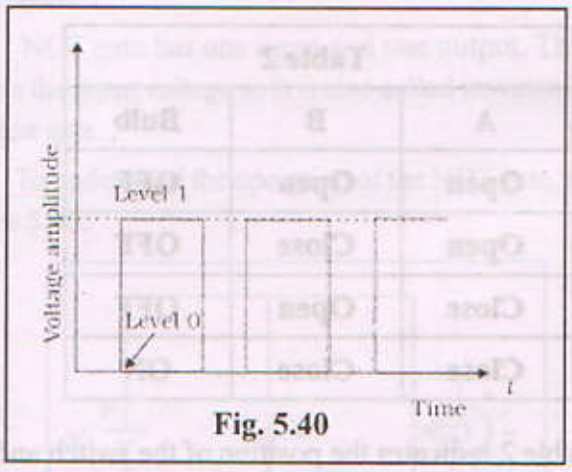


Fig. 5.40

Binary numbers (0 and 1) are used to represent such signals. Only these two levels of voltage are used in digital electronics. Both input and output are either Level 0 or Level 1.

An example of digital signals : When you switch on a light in your house, the output value is state 1 which turns the light ON. When you switch it off, the output value drops to state 0, switching the light OFF.

Simply, digital signal is either a YES or NO, nothing in between.

In digital circuits,

State 0 = No, False, Switch Off, Open Circuit, and Low.

State 1 = Yes, True, Switch On, Closed Circuit, and High.

Logic Gates process digital signals in a specific manner and are used in calculators, digital watches Microprocessors, etc. Let's understand them better.

Let us get familiarized with some of the terms used in digital electronics.

Logic Gate :

The logic circuit in which there is one or more than one input but only one output is called a logic gate. Its output has only two states, '0' or '1', which depends on condition of input signal.

Logic gates are basic building blocks from which most of the digital systems are build up. They are called logic gates as they control the flow of information.

There are 3 types of logic gates–

(1) Basic Gates : OR, AND, and NOT Gates.

(2) Universal Gates : NAND, and NOR Gates.

(3) Derived Gates : XOR Gates, and XNOR Gates.

Boolean Equation : The Boolean equation represents the special type of algebraic representation, which describes the working of the logic gates.

Truth Table : The table which indicates the output for different combinations of the input voltage is known as the truth table. Truth tables help understand the behaviour of logic gates.

Now, let us discuss about the Logic gates come under each category one by one.

Basic Gates :

OR gate :

The **figure 5.41** shows the circuit containing the bulb and the two switches A and B to illustrate the working of an OR gate.

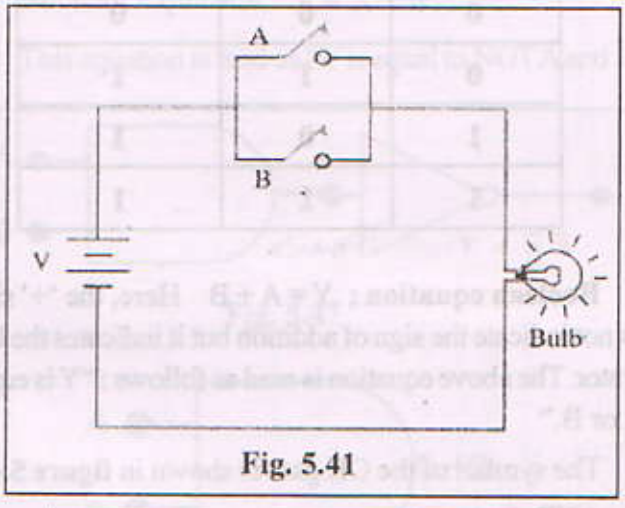


Fig. 5.41

Table 1		
A	B	Bulb
Open	Open	OFF
Open	Close	ON
Close	Open	ON
Close	Close	ON

When any one of the switches or both the switches will be ON, then bulb will be ON. When both switches will be OFF then bulb will remain OFF.

The status of the bulb with respect to the switch positions is shown in table 1. In this table if the switch A is taken as input A the switch B is taken as input B and the status of the bulb is taken as output Y, we get the truth table of an OR gate.

In this table the ON state is taken as '1' and off state is indicated as '0'. We can describe the characteristics of the OR gate based on the above truth table. Whenever any one input or both the inputs are '1', then we get output "1".

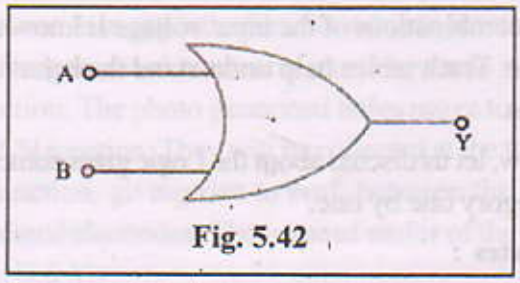


Fig. 5.42

Truth Table for OR Gate		
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

Boolean equation : $Y = A + B$ Here, the '+' sign does not indicate the sign of addition but it indicates the OR operator. The above equation is read as follows : "Y is equal to A or B."

The symbol of the OR gate is shown in **figure 5.42.**

AND Gate :

The **figure 5.43** shows the circuit containing the bulb and the two switches A and B to illustrate the working of an AND gate. Here, the two switches A and B are connected in series with the bulb. Therefore, when any one of the switches will be OFF, current will not flow in the circuit and bulb will remain OFF. When both switches will be ON then only bulb will be ON.

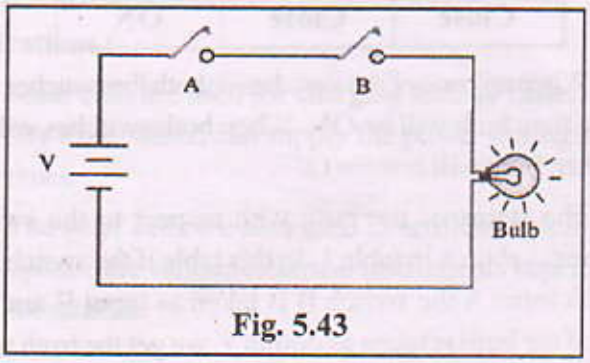


Fig. 5.43

Table 2		
A	B	Bulb
Open	Open	OFF
Open	Close	OFF
Close	Open	OFF
Close	Close	ON

Table 2 indicates the position of the switch and its corresponding state of the bulb. The truth table of the AND circuit can be prepared from this table as follows.

Truth Table for AND Gate		
A	B	Y = A • B
0	0	0
0	1	0
1	0	0
1	1	1

From the truth table, function of the AND gate can be defined as follows.

The output of the AND gate is '1' only if all the inputs are '1'. For all other conditions of the input, is "0".

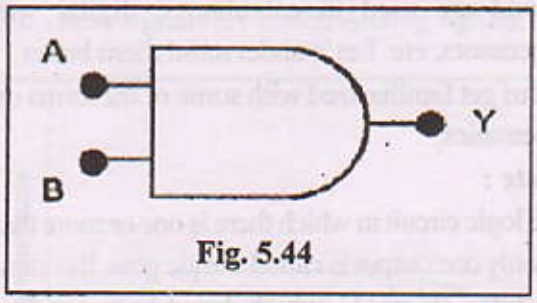


Fig. 5.44

The Boolean equation is given as $Y = A \cdot B$.

Here " • " is known as AND operator. The equation is read as "Y is equal to A AND B".

The symbol of the AND gate is shown in **figure 5.44.**

NOT Gate :

NOT gate has one input and one output. This gate inverts the input voltage so it is also called inverter. This is simplest gate.

To understand the operation of the NOT gate, refer to **figure 5.45.**

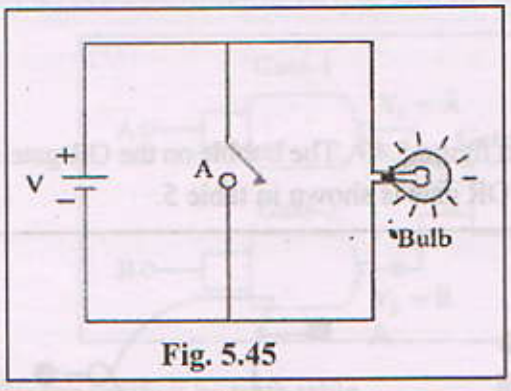


Fig. 5.45

Table 3	
A	Bulb
Open	ON
Close	OFF

Truth Table for NOT Gate	
A	$Y = \bar{A}$
1	0
0	1

When the switch A is open, the current flows through the bulb and the bulb is in ON state. When the switch A is closed no current flows through the bulb and the bulb is in the OFF state. The working of this circuit is summarized in table 3. It is evident from the table 3 that the output reverses the input state. The truth table of the NOT gate is shown above.

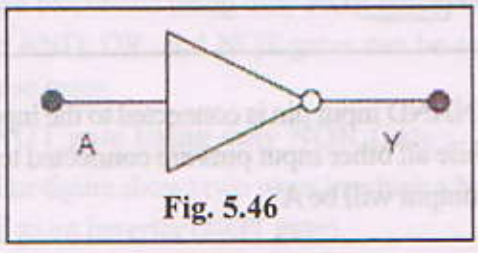


Fig. 5.46

From the truth table, function of the gate can be defined as follows.

"Whenever input is '1' the output is '0' and when the input is '0' the output is '1'."

Hence this gate is also called the inverter.

Boolean Equation : $Y = \bar{A}$. The NOT operator is indicated by the '–' (bar) symbol. The above equation is read as follows : "Y is equal to NOT A."

The AND, OR and NOT logic gates are called the basic logic gates in digital electronics. These gates can be combined in different ways to construct newer logic gates. We shall now study two such logic gates.

Universal Gates :

NAND Gates :

A NAND Gate is a combination of AND Gate and NOT Gate. It is called NAND as N stands for NOT, meaning a NOT AND Gate. For two or more inputs, the output is equal to '1' when any one input is equal to '0' and the output is equal to '0', when all the inputs are equal to '1'.

As shown in **Fig. 5.47**, the output of the AND gate is given as input to the NOT gate. The Boolean expression is given as follows :

Boolean Equation : $Y = \overline{A \cdot B}$

This equation is read as "Y is equal to NOT A and B."

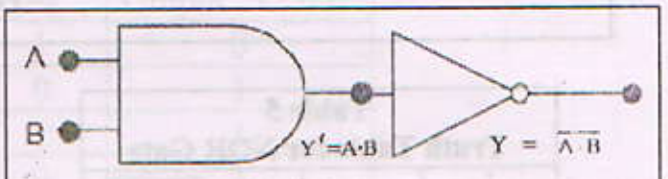


Fig. 5.47

Fig. 5.48

Table 4 Truth Table for NAND Gate			
A	B	$Y' = A \cdot B$	$Y = \overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

The circuit diagram and the symbol of the NAND gate is given in **figure 5.47** and **figure 5.48.** The bubble on the AND gate indicates that the output of the AND gate gets inverted. The truth table of the NAND gate is shown in table 4.

NOR Gates :

A NOR Gate is a combination of OR Gate and NOT Gate. It is called NOR as N stands for NOT, meaning a NOT OR Gate. For two or more inputs, the output is '0' whenever any one input is '1'. Whenever all the inputs are '0', the output is equal to '1'.

As shown in figure 5.49 the output of the OR gate is given as input to the NOT gate. The Boolean expression for the NOR gate is given as follows.

Boolean Equation : $Y = \overline{A + B}$

This equation is read as : "Y is equal to NOT A or B."

The circuit diagram of the NOR gate and its symbol is shown in figure 5.49 . The bubble on the OR gate indicates that the output of the OR gate gets inverted. The truth table of the NOR gate is shown in table 5.

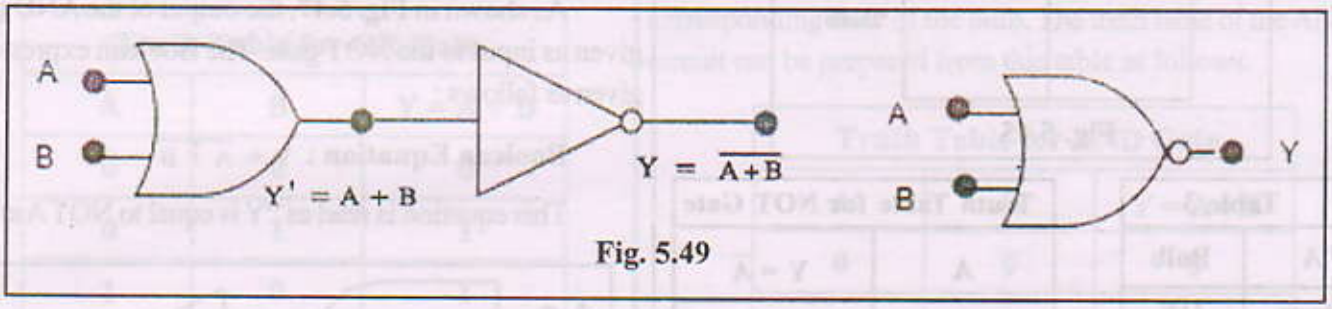


Fig. 5.49

Table 5
Truth Table for NOR Gate

A	B.	A+B	Y= $\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. It means that all other gates can be created from it. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

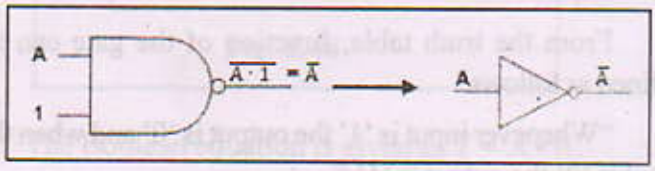
NAND Gate is a Universal Gate : To prove that any gates can be created using only NAND gates, we will show that the AND, OR, and NOT gates can be created using only these gates.

NOT gate using only NAND Gate :

The figure shows two ways in which a NAND gate can be used as an inverter (NOT gate).

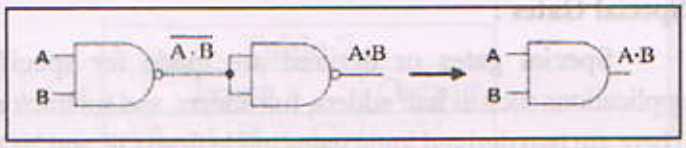
1. All NAND input pins connect to the input signal A gives an output.

2. One NAND input pin is connected to the input signal A while all other input pins are connected to logic 1. The output will be A'.



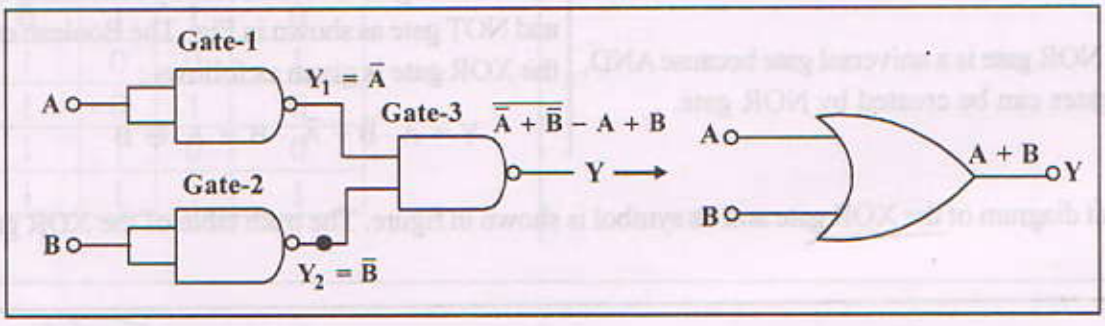
AND gate using only NAND Gates

An AND gate can be created by NAND gates as shown in the figure. Here output of NAND gate is connected as input to a NAND gate inverter.



OR gate using only NAND Gates :

An OR gate can be created by NAND gates as shown in the figure. The OR gate is created by a NAND gate with all its inputs complemented by NAND gate inverters.



We can verify it by truth table.

Input A	Input B	$Y_1=\overline{A}$	$Y_2=\overline{B}$	Output $Y = \overline{Y_1 \cdot Y_2}$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

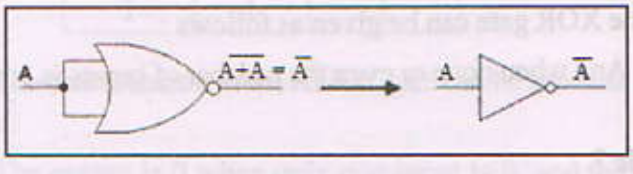
Thus, the NAND gate is a universal gate because AND, OR and NOT gates can be created by NAND gate.

NOR Gate is a Universal Gate : To prove that any gates can be created using only NOR gates, we will show that the AND, OR, and NOT gates can be created using only these gates.

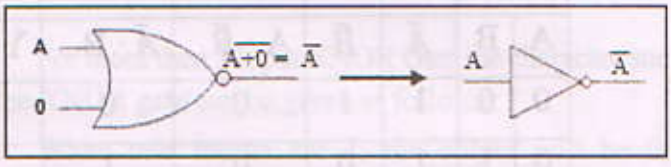
NOT gate Using only NOR Gate :

The figure shows two ways in which a NOR gate can be used as an inverter (NOT gate).

1. All NOR input pins connect to the input signal A gives an output A'.



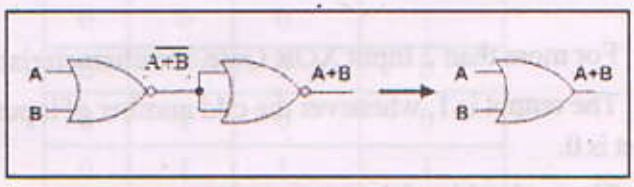
2. One NOR input pin is connected to the input signal A while all other input pins are connected to logic 0. The output will be $\overline{A}$.



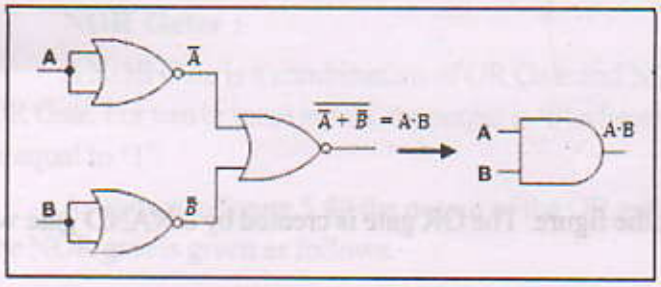
We can verify above using Truth Table.

OR gate using only NOR Gates :

An OR gate can be created by NOR gates as shown in the figure. Here output of NOR gate is connected as input to a NOR gate inverter.



An AND gate can be created by NOR gates as shown in the figure (The AND gate is created by a NOR gate with all its inputs complemented by NOR gate inverters.)



Thus, the NOR gate is a universal gate because AND, OR and NOT gates can be created by NOR gate.

Special Gates :

Special gates or derived are made for specific applications such as half adders, full adders, and subtractors. There are two derived logic gates made from OR and NOR gates.

XOR Gate (Exclusive OR, EX-OR Gate) :

XOR gate is constructed by combining the OR, AND and NOT gate as shown in Fig. The Boolean expression for the XOR gate is given as follows :

$$Y = A \cdot \bar{B} + \bar{A} \cdot B = A \oplus B$$

The circuit diagram of the XOR gate and its symbol is shown in figure. The truth table of the XOR gate is shown in table 6.

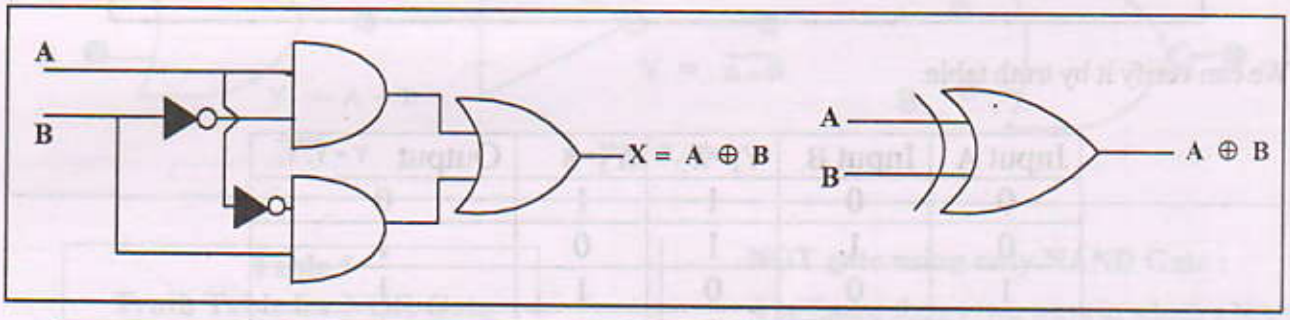


Table 6

Input						Outpt
A	B	$\bar{A}$	$\bar{B}$	$A \cdot \bar{B}$	$\bar{A} \cdot B$	$Y = A \cdot \bar{B} + \bar{A} \cdot B = A \oplus B$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

The characteristic of the XOR gate can be given as follows :

The output is '1' whenever only one input is 1. When both inputs are equal, either '0' or "1" the output is equal to '0'.

For more than 2 Input XOR Gate, the characteristic of the XOR gate can be given as follows :

The output is 1, whenever the odd number of inputs is 1. And when none or even the number of inputs is 1, the output is 0.

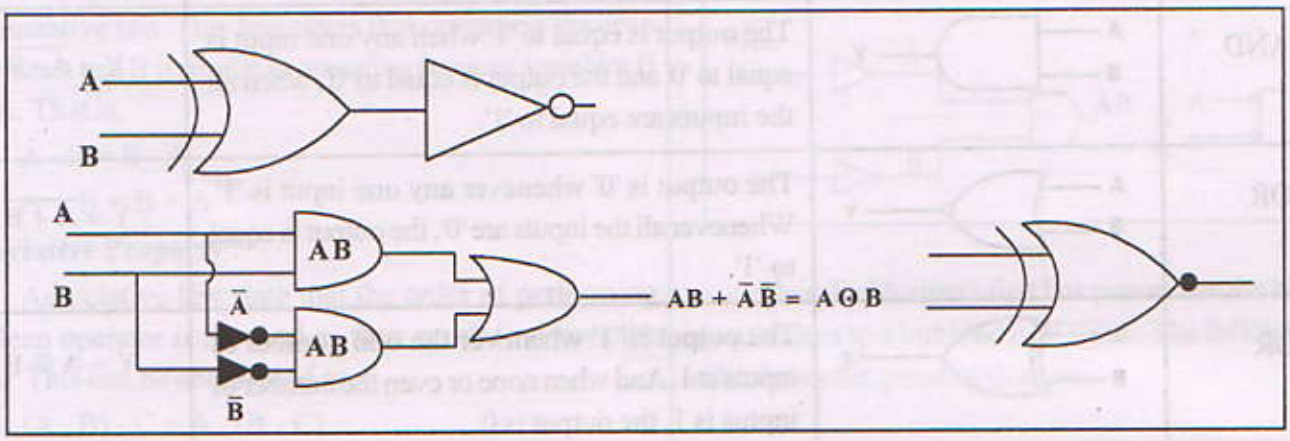
The truth table of the 3 inputs XOR gate is shown in table 7.

Table 7			
Input			Output
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

XNOR Gate :

XNOR gate is a combination of XOR gate and NOT gate. (XOR + NOT = XNOR). The Boolean expression for the XNOR gate is given as follows :

$$Y = A \odot B = A \cdot B + \bar{A} \cdot \bar{B} = \overline{A \oplus B}$$



The circuit diagram of the XNOR gate and its symbol is shown in above figure. The truth table of the XNOR gate is shown in table 8.

Table 8		
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

The characteristic of the XNOR gate can be given as follows:

The output is 0 when only one input is 0, and the output is 1 when both inputs are the same (i.e., two 0's or two 1's).

For more then 2 Input XNOR Gate the characteristic of the XNOR gate can be given as follows :

When odd inputs are 1, the output will be 0; otherwise, it will be 1.

The truth table of the 3 inputs XNOR gate is shown in table 9.

Table 9			
Input			**Output**
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	1	0	1
1	1	1	0

- **Summary of Logic Gates :**

Logic Gate	Symbol	Description	Boolean
AND		The output of the AND gate is '1' only if all the inputs are '1'. For all other conditions of the input, is "0".	$Y = A \cdot B$
OR		Whenever any one input or all the inputs are '1' then we get output "1". And when all the inputs are '0' then we get output "0".	$Y = A + B$
NOT		Whenever any one input or all the inputs are '1' then we get output "1". And when all the inputs are '0' then we get output "0".	$Y = \bar{A}$
NAND		The output is equal to '1' when any one input is equal to '0' and the output is equal to '0', when all the inputs are equal to '1'.	$Y = \overline{A \cdot B}$
NOR		The output is '0' whenever any one input is '1'. Whenever all the inputs are '0', the output is equal to '1'.	$Y = \overline{A + B}$
XOR		The output is '1' whenever the odd number of inputs is 1. And when none or even the number of inptus is 1, the output is 0.	$Y = A \oplus B$
XNOR		When odd inputs are 1, the output will be 0; otherwise it will be 1.	$Y = \overline{A \oplus B}$

5.13 Boolean Algebra :

Boolean algebra is a branch of algebra that involves variables that have two possible values : true (1) and false (0). It is also called Binary Algebra or logical Algebra. It is the foundation of digital logic design and is widely used in computer science, electrical engineering and mathematics.

Basic Boolean Operations :

The basic Boolean operations are explained below with their expressions :

1. AND Operation :

The AND operation is denoted by a dot (·). It returns true only if both variables are true (1).

$A \cdot B = B \cdot A$

2. OR Operation :

The OR operation is denoted by a plus sign (+). It returns true (1) if at least one of the operands is true (1).

$A + B = B + A$

3. NOT Operation (Negation) :

The NOT operation is denoted by an over line ($\bar{A}$). It inverts the value of the operand.

Some properties of Boolean algebra.

Identity Law :

In the Boolean Algebra, we have identity elements for both AND (•) and OR (+) operations. The identity law state that in Boolean algebra we have such variables that on operating with AND and OR operation we get the same result, i.e.

$A \cdot 1 = A$

$A + 0 = A$

In Boolean Algebra, both AND (·) and OR(+) perations have a **Identity elements.** If one of the two puts of an AND (•) gate is 1, its output is the same as the her input, so 1 is the Identity element of the AND (•) gate.

$A \cdot 1 = A$

If one of the two inputs of an OR (+) gate is 0, its utput is the same as the other input, so 0 is the Identity lement of an OR (+) gate.

$A + 0 = A$

Commutative Law :

Binary variables in Boolean algebra follow the ommutative law. This law states that operating Boolean ariables A and B is similar to operating Boolean variables B nd A. That is,

$A \cdot B = B \cdot A$

$A + B = B + A$

Associative Property :

Associative law state that the order of performing Boolean operator is illogical as their result is always the ame. This can be understood as,

$(A \cdot B) \cdot C = A \cdot (B \cdot C)$

$(A + B) + C = A + (B + C)$

Distributive Property :

Boolean Variables also follow the distributive law and he expression for Distributive law is given as :

$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$

Inversion Law :

Inversion law is the unique law of Boolean algebra. This law states that, the complement of the complement of any number is the number itself.

$\overline{\overline{A}} = A$

Other Property of Boolean algebra :

	AND (•)	OR (+)
1	$A \cdot A = A$	$A + A = A$
2	$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$
3	$A \cdot 0 = 0$	$A + 0 = A$
4	$A \cdot 1 = A$	$A + 1 = 1$

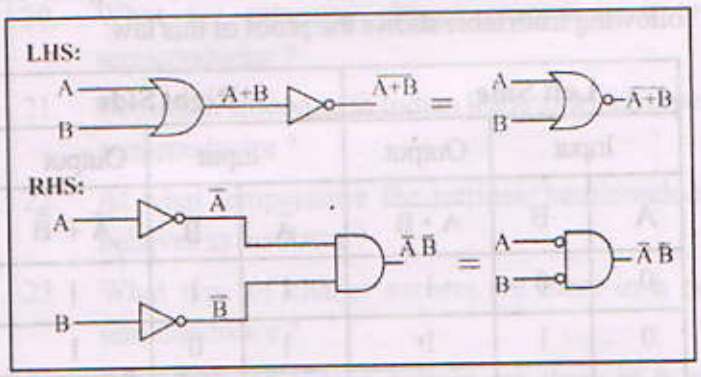
5.14 DeMorgan's Laws :

DeMorgan's First Law :

The complement of two or more ORed variables is equivalent to the AND of the complements of each of the individual variables, i.e.

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

The logic implementation of left side and right side of this law is shown in **Figure 5.50.**



Thus, DeMorgan's first law proves that the NOR gate is equivalent to a bubbled AND gate. The following truth table shows the proof of this law.

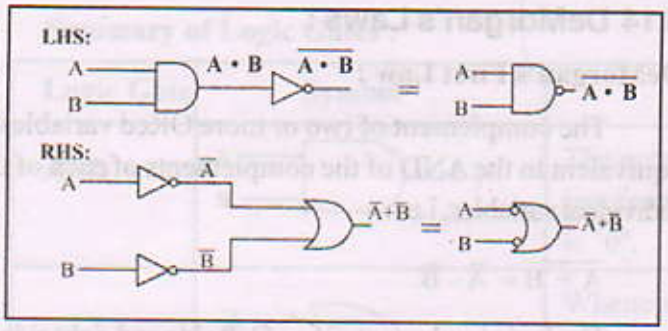
Left Side			Right Side		
Input		Output	Input		Output
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

DeMorgan's Second Law :

The complement of two or more ANDed variables is equal to the sum of the complement of each of the individual variables, i.e.,

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

The logic implementation of left and right sides of this expression is shown in Figure.



Hence, DeMorgan's second law proves that the NAND gate is equivalent to a bubbled OR gate. The following truth table shows the proof of this law.

Left Side			Right Side		
Input		Output	Input		Output
A	B	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

EXERCISE

1. Explain : (1) Conductors, (2) Insulators, (3) Intrinsic semiconductors.
2. Write electronic configuration of silicon (Si).
3. Explain the concept of Hall in a semiconductor.
4. Explain with diagram how electrons and holes conduct electricity in pure or intrinsic semiconductors.
5. How are N-type semiconductors prepared ? Who are the majority charge carriers in this type of semiconductor ?
6. Write a short note on P-type semiconductor.
7. Write four points of difference between P-type and N-type semiconductors.
8. Explain the electrical conduction in intrinsic semiconductor with the help of band diagram.
9. Explain energy band diagram for insulators and conductors.
10. Draw and explain the energy band diagram of N - type semiconductor for 0 K temperature and room temperature.
11. Draw and explain the band diagram for a p-type semiconductor at 0 K temperature and room temperature.
12. What is a P-N junction diode ? Explain the diffusion process taking place near the junction during formation of the junction. Is this process continuous ?
13. Explain the depletion layer and depletion barrier of a P-N junction diode with necessary diagram.
14. Draw the circuit diagram to obtain forward bias characteristics of a P-N junction and discuss the forward bias characteristics of it.
15. Draw a characteristic of forward bias graph for a P-N junction diode. How can the dynamic reistance of the diode be found from this ?
16. Draw the electrical circuit diagram to obtain the reverse bias characteristic for a P-N junction diode and discuss its reverse bias characteristic graph.
17. Write four points of difference between forward bias and reverse bias characteristics of P-N junction diode.
18. What is rectification and rectifier ? A P-N junction diode can be used as a rectifier. Explain it in brief based on appropriate discussion.
19. Draw the circuit of half wave rectifier and explain its working. Also draw the input voltage and output voltage waveforms for this circuit.
20. Using two diode draw the electric circuit of full wave rectifier. Through this circuit, explain how the voltage at the output is found during both half-cycles of the a.c input voltage.
21. Write three points of difference between half wave rectifier and full wave rectifier.
22. Explain the working of a OR gate. Give the symbol, Boolean expression and truth table of a OR gate.
23. Explain the working of a AND gate. Give the symbol, Boolean expression and truth table of a AND gate.
24. Explain the working of a NAND gate. Give the symbol, Boolean expression and truth table of a NAND gate.
25. Explain the working of a NOR gate. Give the symbol, Boolean expression and truth table of a NOR gate.